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Kaushik Vaidyanathan received a B.E. degree in Electronics and Communication Engineering from the Madras Institute of Technology at Chennai, India, and M.S. and Ph.D. degrees in Electrical and Computer Engineering from Carnegie Mellon University (CMU), Pittsburgh, PA. He started as an application-specific integrated circuit (ASIC) physical-design engineer at IBM in 2007. Subsequently, in 2009, he started his Ph.D. research under the supervision of Prof. Larry Pileggi at CMU, exploring design techniques that enable cost-effective and efficient SoC design below N20. Along with his collaborators at IBM and CMU he developed the holistic design technology co-optimization process and demonstrated its efficacy at N14. First as a Ph.D. student and then a postdoc at CMU, he and his collaborators developed a split-fabrication-based design flow to manufacture trusted integrated circuits. Since 2015, Dr. Vaidyanathan works as a Research Scientist at Intel Labs, where he explores the implications of using emerging devices, interconnects, and process integration methods on microprocessor and system-on-chip designs.



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