Extending the Era of Moore's Law

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ABSTRACT

The virtuous cycle of integrated-circuit (IC) technology advancement has resulted in the proliferation of information and communication technology with revolutionary economic and social impact. Advancements in lithography have been critical to sustaining Moore's law over the past 50+ years. As the minimum feature size of an IC has been scaled down well below the wavelength of light used in the photolithographic process, however, the semiconductor industry has faced a growing challenge of continuing to increase the density of transistors at ever lower cost per transistor. This paper discusses a cost-effective method for defining sublithographic features that can help to extend the era of Moore's Law.

Keywords: Technology scaling, sublithographic patterning

1. INTRODUCTION

The proliferation of information and communication technology – which has had dramatic economic and social impact – has been enabled by the steady advancement of silicon-based integrated circuit (IC) technology to follow Moore's Law, which states that the number of transistors on an IC "chip" doubles every two years. Gordon Moore observed in 1965 that "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year…"[1] and he revised the rate in 1975 to be 2× every 2 years. In other words, the primary reason for increasing the number of components (transistors) on a chip is to lower the manufacturing cost per component. Additional benefits of increased integration include improved system performance and improved energy efficiency. The virtuous cycle of IC technology advancement (higher transistor density → lower cost and better performance → semiconductor market growth → technology advancement → higher transistor density, *etc*.) has been sustained for more than 50 years, so that the most advanced chips today comprise over 20 billion transistors. Evolution of the conventional planar metal-oxide-semiconductor field-effect transistor (MOSFET) structure into the non-planar multi-gate FinFET[2] structure has facilitated scaling to gate lengths below 25 nm; transistors with gate length as small as 1 nm have been experimentally demonstrated.[3] The pace of increasing transistor count may slow down dramatically, however, due to fundamental limits of the conventional photolithographic patterning process which make it difficult to continue to increase the density of features within an IC layer to increase the density of transistors on a chip.

Photolithographic patterning involves 4 processes: (1) coating of a light-sensitive organic material called photoresist, (2) light exposure through a mask followed by immersion in a chemical developer solution to reproduce the mask pattern in the photoresist layer, (3) selective etch to transfer the pattern from the photoresist layer into the IC layer, and (4) selective removal of the photoresist layer. For layers with critical dimensions, a hard (inorganic) masking material is used to pattern the IC layer with better etch selectivity; in this case, extra processes are required to deposit the hard mask layer prior to photoresist coating, to etch the hard mask layer according to the pattern of the developed photoresist layer, and to remove the hard mask layer after it is used to pattern the IC layer, *i.e.* 7 processes are needed. "Blurring" of the pattern on the wafer produced by the exposure process worsens as the size of the features shrinks further below the wavelength of the light, which is 193 nm for the most advanced exposure tools used in high-volume IC manufacturing today. The more complex the shape of a sub-wavelength feature, the more difficult it is to print with good fidelity. For example, "two-dimensional" features that have serifs such as brackets ([ ) or bends such as in the letter "L" or zig-zags (┌┘) are much more difficult to print than "one-dimensional" (1D) features, *i.e.* straight lines, due to more complex diffraction effects. Therefore, for the most advanced chips produced today, the densest IC layer patterns are restricted to comprise only linear features, often with uniform pitch. The minimum pitch ($P_{\min}$) of features defined by photolithography is limited by diffraction and is proportional to the wavelength of light, λ:

$$P_{\min} = {2k_1\lambda}\Big/{n_i(\sin\theta)} \quad (1)$$

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where k_1 is a process factor with a physical lower limit of 0.25, θ is the propagation angle of the projection lens system (typically ~70°), and n_i is the lowest index of refraction of the propagation medium. For a state-of-the-art 193 nm water-immersion (n_i = 1.44) exposure tool, P_{min} is roughly 90 nm.

2. DOUBLE-PATTERNING TECHNIQUES

Due to the low transmittance of blank mask materials and/or the limited availability of high-intensity light sources for wavelengths shorter than 193 nm, the semiconductor industry has resorted to "double-patterning" techniques to increase the density of linear features patterned in an IC layer on a chip. One such technique is referred to as "double exposure, double etch" or "litho-etch-litho-etch (LELE)." As implied by its name, it involves roughly twice the number of processes as the conventional process to pattern a single IC layer, as shown in Figure 1.

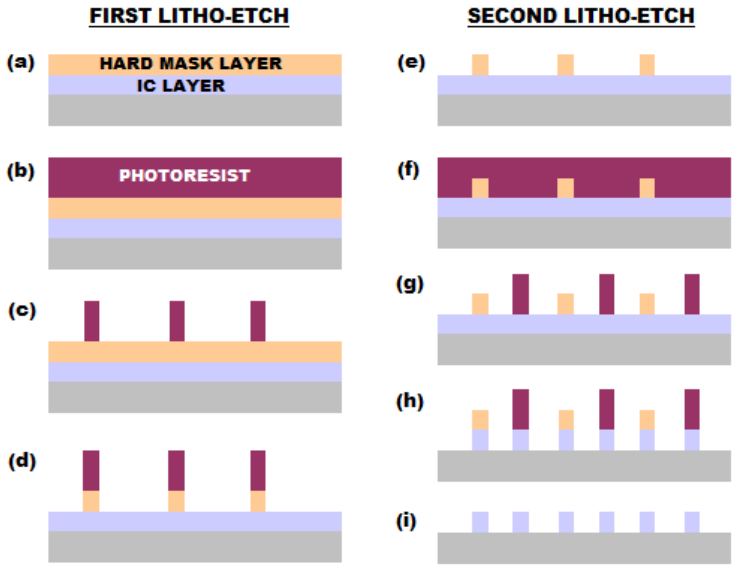

Figure 1. Schematic cross-sections illustrating the litho-etch-litho-etch (LELE) double patterning technique: (a) the IC layer to be patterned is coated with a hard mask layer; (b) a first layer of photoresist is coated onto the hard mask layer; (c) photolithography is used to print features in the photoresist layer – note that these usually are "trimmed" to become narrower than the lithographic resolution limit; (d) an etch process is used to remove regions of the hard mask layer in regions not protected by the photoresist; (e) photoresist is selectively removed; (f) a second layer of photoresist is coated; (g) photolithography is used to print features in the photoresist layer – inevitably misaligned with the features patterned using the first photoresist layer; (h) an etch process is used to remove regions of the IC layer not protected by either the hard mask or photoresist; (i) hard mask and photoresist layers are selectively removed.

Another double-patterning technique is referred to as "spacer lithography" or "self-aligned double patterning (SADP)" and is used today in the manufacture of non-volatile memory chips[4] and leading-edge microprocessors[5] with sub-45 nm minimum pitch. It involves even more processes than LELE, as can be seen from Figure 2. In addition, it requires extra lithography and etching processes to eliminate the portions of the spacers located at the ends of the sacrificial linear features (called "mandrels"); otherwise, the spacers formed along the sidewalls of the same mandrel feature would be interconnected.

Iterative double-patterning eventually will be needed to achieve ever higher feature density. Escalating cost due to extra lithography, deposition and etch processes (each of which involve multiple steps, *e.g.* anti-reflection coating, bake, pre-clean, *etc.*) associated with multiple-patterning techniques threaten to bring Moore's Law to an end. Clearly, lower-cost approaches to defining sublithographic features (*i.e.*, smaller than the resolution limit of photolithography) are needed.

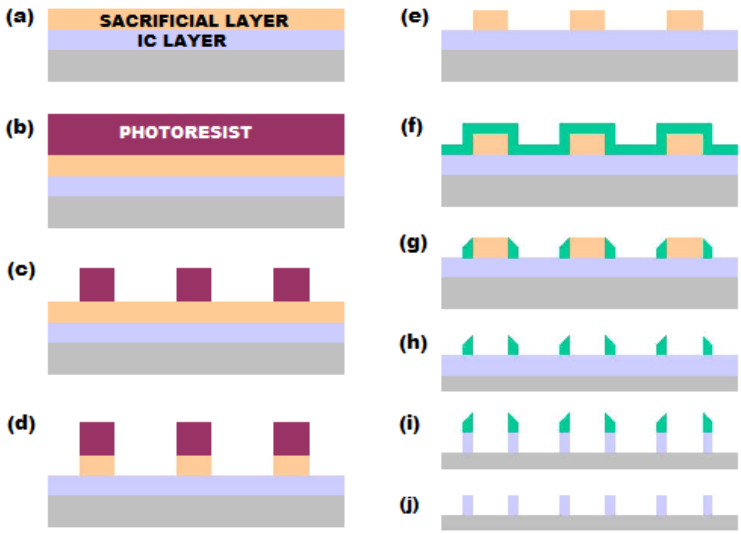

Figure 2. Schematic cross-sections illustrating the self-aligned double patterning (SADP) technique: (a) the IC layer to be patterned is coated with a sacrificial layer; (b) photoresist is coated onto the sacrificial layer; (c) photolithography is used to print features in the photoresist layer; (d) an etch process is used to remove regions of the sacrificial layer in regions not protected by the photoresist; (e) photoresist is selectively removed; (f) a relatively thin hard mask layer is conformally deposited; (g) an anisotropic etch process is used to form hard-mask "spacers" along the sidewalls of the sacrificial layer patterns – note that the width of these spacers is correlated with the thickness of the deposited hard mask layer, and can be much smaller than the lithographic resolution limit; (h) the sacrificial layer is selectively removed; (i) an etch process is used to remove regions of the IC layer not protected by the spacers; (j) the spacers are selectively removed.

It is worthwhile to note here that directed self-assembly (DSA) of a diblock copolymer film[6] has been proposed as a sublithographic patterning technique: the film is coated onto a wafer with lithographically defined features on its surface, which serve as a guide for the formation of the sublithographic features; self-assembly (phase separation) occurs upon heating to form features as small as a few nanometers, depending on the degree of polymerization (number of monomer repeats in the chain) and the block-block interaction parameter. Although this technique shows promise for patterning sub-20 nm contact holes for practical ICs,[7] it has a number of drawbacks for patterning linear features include a limited range of feature widths and pitches for a given diblock copolymer material formulation, and line-edge roughness (LER) which does not scale well with the line width.

3. TILTED ION IMPLANTATION ENHANCED PATTERNING

Ion implantation is a standard technique used in IC manufacturing to introduce impurity atoms in precise amounts (doses in the range from $10^{11}/cm^2$ to $10^{16}/cm^2$) into the surface region of the wafer, over a range of depths. The projected range and straggle of the implanted ions is determined by the implant energy, which can range from less than 1 keV to 60 keV in common implanters, as well as by the properties of the implanted material. The implant tilt angle (*i.e.*, angle of incidence) can be readily adjusted in the range from -60^o to $+60^o$. To address the challenge of escalating IC manufacturing cost, a double-patterning method that utilizes tilted ion implantation (TII) recently was proposed and demonstrated to be suitable for achieving linear feature sizes below 10 nm.[8] As illustrated in Figure 3, this new approach only requires one additional process (TII) in comparison with a conventional (photolithography + hard mask) patterning process, to double the feature density. It leverages the fact that the wet etch rate of silicon-dioxide (SiO_2) can be significantly enhanced by implant-induced damage,[9] together with the shadowing effect of masking features (formed prior to TII) on the surface of the wafer. Note that the TII-defined sublithographic features are self-aligned to the pre-existing masking features and that their widths can be easily fine-tuned by adjusting the implant tilt angle. Due to lateral straggle of the implanted ions and the isotropic nature of the hard mask wet etching process, LER of a TII-defined edge is lower than that of its corresponding pre-existing mask feature edge.[10]

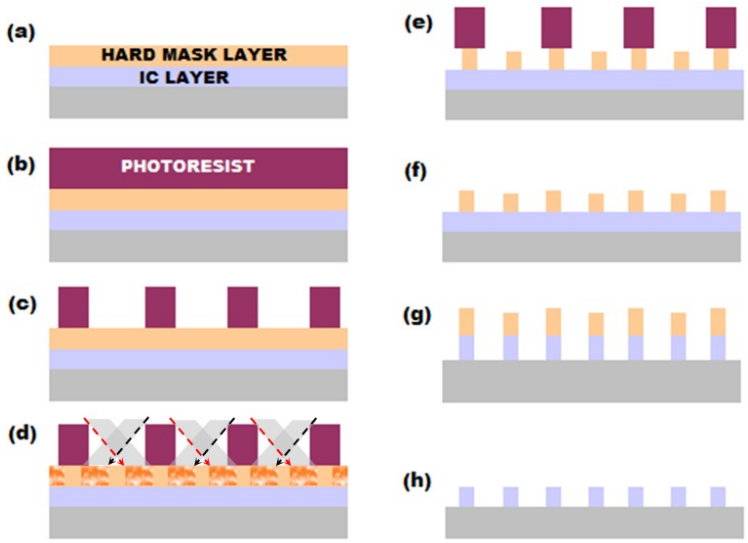

Figure 3. Schematic cross-sections illustrating the tilted ion implantation double patterning technique: (a) the IC layer to be patterned is coated with a hard mask layer; (b) photoresist is coated onto the hard mask layer; (c) photolithography is used to print features in the photoresist layer; (d) ion implantation is performed at positive (black dashed lines) tilt angle and also at negative (red dashed lines) tilt angle to selectively damage regions of the hard mask layer, leaving the central region between the photoresist features undamaged due to the shadowing effect; (e) portions of the hard mask layer which are damaged are etched away more rapidly than undamaged portions, by wet etching; (f) the photoresist layer is removed; (g) an etch process is used to transfer the pattern of the hard mask to the IC layer; (h) hard mask layer is selectively removed.

Ion implantation is a relatively simple process as compared to lithography, deposition, and etch processes, since it does not require steps to pre-coat, pre-clean, or pre-bake the wafer. Therefore, the cost of TII double-patterning can be substantially lower than the cost of SADP, as shown in Table 1. It should be noted that TII can be used together with masking features formed by SADP to further double the feature density (achieving < 25 nm pitch).

Table 1. Cost comparison of double patterning approaches (adapted from [11]).

Self-Aligned Double Patterning			**TII Double Patterning**		
Sequence of Fabrication Processes		**Cost**	**Sequence of Fabrication Processes**		**Cost**
Process	**Description**	**(a.u.)**	**Process**	**Description**	**(a.u.)**
PECVD	Etch-stop layer	1.5	PECVD	Hard mask layer	2
CVD	Mandrel layer deposition	2	Photolithography	Pattern definition	30
Photolithography	Pattern definition	30	Implantation	Tilted implants	1.7
RIE	Mandrel etch	10	Wet etch	Hard mask etch	1
ALD	Spacer deposition	3	RIE	Pattern transfer to IC layer	16
RIE	Spacer etch	16	Wet etch	Hard mask removal	1
Wet etch	Mandrel removal	1			
RIE	Pattern transfer to IC layer	16			
Wet etch	Spacer removal	1			
Wet etch	Etch stop layer removal	1			
	Total:	**81.5**		**Total:**	**<52**

CVD: Chemical Vapor Deposition; PECVD: Plasma Enhanced CVD; RIE: Reactive Ion Etching; ALD: Atomic Layer Deposition

TII also can be used to achieve non-linear features, if the pre-existing masking features are not linearly shaped. For example, sub-20 nm holes have been experimentally demonstrated.[8] By using multiple masking steps together with multiple TII steps, two-dimensional (2D) patterns with minimum pitch smaller than P_{min} and with minimum feature size smaller than the lithographic resolution limit ($P_{min}/2$) should be achievable. More specifically: multiple lithography processes, each followed by a TII process, can be used to create a latent 2D pattern in a hard mask layer; subsequently the pattern in the hard mask can be "developed" by etching the hard mask material selectively in the implanted regions; afterwards the pattern is transferred to an underlying IC layer by an etch process. Figures 4(a)-4(c) show plan-view schematics of an exemplary 2D pattern, how it can be formed from a combination of overlaid 1D patterns, and a corresponding set of dark-field lithographic mask features (*i.e.* corresponding to the rectangular regions from which photoresist is to be removed in developer solution) that can be used to define the 1D patterns via multiple lithography+TII sequences. (The ion trajectory direction is indicated by the arrows, according to the line type for each dark-field mask feature.) Note that at each right-angle bend in the 2D pattern, the orthogonal 1D pattern features comprising it overlap; the degree of overlap in each direction can be adjusted in practice to minimize unwanted blurring or bloating while ensuring a continuous bend.

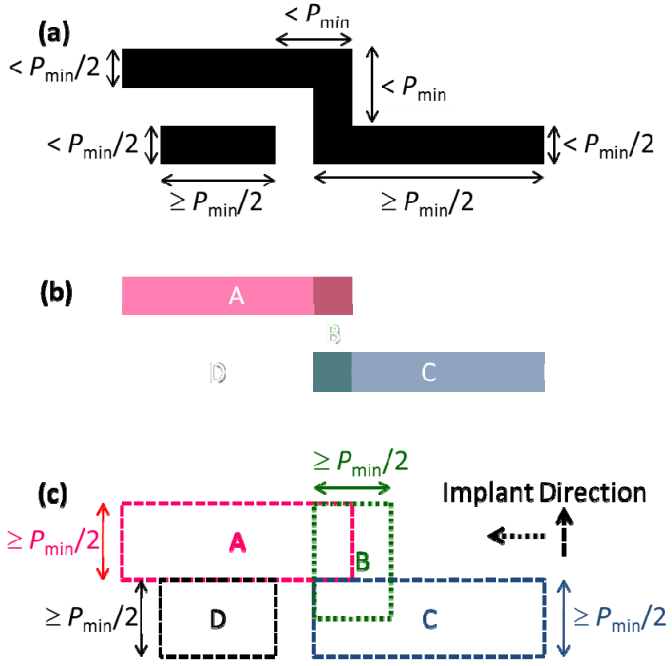

Figure 4. Schematic plan views: (a) an exemplary 2D IC-layer pattern with sub-lithographic features and feature pitch; (b) 1D patterns (labeled A, B, C, D) which when overlaid form the 2D pattern in (a); (c) a corresponding set of dark-field lithographic mask features that can be used in conjunction with tilted ion implantation to generate the four 1D patterns A, B, C, D; the ion trajectory direction is indicated by the arrows, according to the line type for each mask feature.

An IC layer would be 2D-patterned as follows: Firstly a hard mask layer would be deposited onto the IC layer; then lithography+TII would be performed using each of the 4 masks in sequence; afterwards the hard mask would be selectively etched to form the composite 2D pattern, after which the 2D pattern would be transferred to the IC layer by a selective etch process.

4. CONCLUSION

Tilted ion implantation (TII) can be used to pattern features with dimensions below 10 nm and with lower line-edge roughness than that of the pre-existing masking features to which they are self-aligned. With the advantages of lower cost and greater versatility as compared with self-aligned double patterning, TII enhanced patterning shows promise for enabling IC technology scaling beyond the 5 nm node (sub-20 nm pitch), to extend the era of Moore's Law.

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