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*A. M. Aurora*

*V. V. Marochkin*

*T. Tuuva*

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# A NOVEL RADIATION HARD PIXEL DESIGN FOR SPACE APPLICATIONS

A. M. Aurora[1,2], V. V. Marochkin[1,2], T. Tuuva[2]
[1]*Pixpolar, Tekniikantie 1, 02150 Espoo, Finland*
[2]*Lappeenranta University of Technology, P.O. Box 20, 53851 Lappeenranta, Finland*

*Email: artto.aurola@pixpolar.com*

***Abstract* - We have developed a novel radiation hard photon detector concept based on Modified Internal Gate Field Effect Transistor (MIGFET) wherein a buried Modified Internal Gate (MIG) is implanted underneath a channel of a FET. In between the MIG and the channel of the FET there is depleted semiconductor material forming a potential barrier between charges in the channel and similar type signal charges located in the MIG. The signal charges in the MIG have a measurable effect on the conductance of the channel. In this paper a radiation hard double MIGFET pixel is investigated comprising two MIGFETs. By transferring the signal charges between the two MIGs Non-Destructive Correlated Double Sampling Readout (NDCDSR) is enabled.**

**The radiation hardness of the proposed double MIGFET structure stems from the fact that interface related issues can be considerably mitigated. The reason for this is, first of all, that interface generated dark noise can be completely avoided and secondly, that interface generated 1/f noise can be considerably reduced due to a deep buried channel readout configuration.**

**Electrical parameters of the double MIGFET pixel have been evaluated by 3D TCAD simulation study. Simulation results show the absence of interface generated dark noise, significantly reduced interface generated 1/f noise, well performing NDCDSR operation, and blooming protection due to an inherent vertical anti-blooming structure. In addition, the backside illuminated thick fully depleted pixel design results in low crosstalk due to lack of diffusion and good quantum efficiency from visible to Near Infra-Red (NIR) light. These facts result in excellent Signal-to-Noise Ratio (SNR) and very low crosstalk enabling thus excellent image quality. The simulation demonstrates the charge to current conversion gain for source current read-out to be 1.4 nA/e.**

## I. INTRODUCTION

At present there are only two types of widely used image sensor technologies, namely Charge Coupled Device (CCD) and Complementary Metal Oxide Semiconductor (CMOS) image sensors. In both of these technologies an External Gate Readout Configuration (EGRC) is utilized to readout the signal. The external gate readout configuration has, however, major problems hampering the performance in space applications. The most notable one is accumulation of read noise.

In order to perform accurate readout Correlated Double Sampling (CDS) readout has to be used. The problem in EGCR is that the CDS readout is destructive, i.e. the signal is destroyed in the readout process when the signal charge is brought to the external gate. This means that the more often readouts are performed in EGRC the higher the overall read noise and thus the lower the SNR.

In Destructive CDS Readout (DCDSR) one should utilize a long integration time in order to maximize the image quality of faint deep space objects. Correspondingly one should use much shorter integration times in order to detect asteroids and to determine their tracks. In other words, in CCD and CMOS image sensors one cannot use simultaneously optimal settings for both tasks impairing usability of earth and space based astronomical cameras.

It is possible to get rid off the accumulation of read noise by amplifying the signal before readout, which is utilized in amplified image sensors like Electron Multiplication CCDs (EMCCDs) [1]. The problem is, however, that amplification results in amplification noise, which reduces the SNR. In addition there are also other problems in EMCCDs like smear and Clocking Induced Charge (CIC). In Single-Photon Avalanche Diode (SPAD) [2] the amplification noise can be avoided but the problem is poor Fill Factor (FF), dead time, and after pulsing.

It is possible to avoid accumulation of read noise without introducing additional noise through NDCDSR, i.e., through accurate non-destructive signal readout. The NDCDSR has been demonstrated in an Internal Gate Readout Configuration (IGRC) [3]. The problem is, however, very large and unpractical pixel size as well as manufacturability issues. The latter one stems from the fact that in IGRC signal charges modulate an oppositely charged current running in the transistor channel. This means that it is very difficult to match the location of the minimum channel threshold of the readout transistor with the signal charge potential minima leading to poor tolerance against process fluctuations.

It is important to note that although the signal charge is readout CDS wise multiple times in skipper CCD [4] the signal charge will be destroyed after the multiple readouts and thus it does not truly

posses NDCDSR ability.

Yet another problem of EGRC is that it is difficult to mitigate the effect of 1/f noise on the read noise and thus on SNR. By far the major part of the 1/f noise stems from the interface and thus by utilizing a buried channel readout transistor the 1/f noise can be reduced – the deeper the channel the smaller the 1/f noise. However, the deeper the buried channel in EGRC the smaller the signal. Another problem is also that in EGRC the spurious signal due to a charge trapped at the interface beneath the gate is always larger than the signal produced by a signal charge on the sense node and the deeper the buried channel the larger this difference is. A third reason is that the smaller amount of signal charges leads to the shallower buried channel, meaning that the smaller the signal the more there will be 1/f noise. This effect results in also non-linearity issues. These reasons reduce the beneficial effect of a deep buried channel on SNR in EGRC.

In the IGRC of [3] a surface channel readout transistor is utilized resulting in a lot of 1/f noise. The problem is that generally in IGRC a circular readout transistor is more or less mandatory in order to improve the manufacturability but the circular readout transistor inhibits the use of a deep buried channel. One could also reduce 1/f noise by utilizing IGRC in conjunction with a circular JFET design, but it would also worsen the manufacturability.

Yet another problem of the EGRC is interface generated dark noise. In CCD and CMOS image sensors the interface generated dark noise can be effectively mitigated during the integration period with the help of a pinned photo diode design wherein the transfer gate is held at a negative bias during the integration period. The negative transfer gate bias results in, however, blooming unless a buried channel is used either underneath the transfer gate or underneath an extra anti-blooming gate.

By optimizing the manufacturing process to minimize interface leakage and by utilizing a relatively short readout period it is possible to keep the interface dark noise at bay during readout in earth based instruments. In CCD image sensor an extra challenge is to keep the interface induced dark noise at a reasonable level during the transfer period.

In CMOS image sensors there is an additional problem referred to as image lag which stems from trapping and releasing signal charges at interface (and oxide) defects located beneath the transfer gate during signal charge transfer from the pinned photodiode to the floating diffusion. By transferring the signal charges in a deep buried channel during transfer period when transfer gate is at positive potential one could effectively remove the image lag. The problem is, however, that during integration when the transfer gate is at negative bias the buried channel would be even much deeper than during transfer reducing considerably the full well capacity. On the other hand, one would need to use a substantial negative bias on the transfer gate in order to form an inversion layer at the interface preventing the formation of interface dark noise during integration. If the negative bias required to form the inversion layer is more than the gate oxide can endure then one has to sacrifice either image lag or dark noise performance.

In addition, it is very difficult to design a CMOS image sensor featuring CDS readout and having a thick fully depleted substrate. In case of a thick CMOS image sensor this fact means that some of the Quantum Efficiency (QE) for NIR will be lost due to recombination in the neutral bulk and that the crosstalk performance will be very poor. In case of a thin CMOS image sensor one will achieve only very poor QE for NIR but very good crosstalk performance. Furthermore even in Back-Side Illuminated (BSI) CMOS image sensor configuration it is difficult to achieve 100 % fill-factor in a thin sensor design. Thus neither thick nor thin CMOS image sensors are ideal for detecting closely spaced objects and particularly so if the other object were dim like e.g. a planet orbiting a star.

Yet another problem in CMOS image sensors is that voltage mode readout (aka source follower readout) is typically preferred due to the fact that the smaller the overall capacitance of the sense node the bigger the signal. In the current mode readout the signal size depends on the on sense node's readout (i.e. readout transistor's gate to channel capacitance) to parasitic capacitance ratio. This fact effectively prevents the use of a deep buried channel readout transistor in CMOS image sensors utilizing current mode readout. The problems in the voltage mode readout are, on the other hand, the fact that the charging of the long source line creates an RC delay and more importantly capacitive coupling of the long source lines to the sense nodes of other pixels in the same row being simultaneously readout. The latter fact substantially increases the cross-talk between pixels.

The problem in space is that an image sensor suffers from radiation damage increasing the noise and limiting the lifetime of the sensor. The radiation damage induced noise comprises two basic components, interface and bulk generated noise.

In EGRC the interface (and oxide) induced radiation damage in space increases the 1/f noise and dark noise during readout relatively fast to a much higher level than on earth. Furthermore in CMOS image sensors excess radiation induced image lag will be easily introduced and in CCDs radiation induced interface dark noise may increase very rapidly due to the relatively long transfer period. Thus the interface (and oxide) based radiation damage shortens the useful lifetime of

space based CCD and CMOS image sensors.

Thick fully depleted BSI deep buried channel double MIG image sensors have several benefits. They offer NDCDSR, interface generated dark noise and image lag free operation, very low 1/f noise, 100 % fill factor, excellent QE for both NIR and visible light, very low crosstalk, inherent vertical anti-blooming mechanism, very fast operation, as well as good manufacturability with existing CMOS manufacturing lines.

The good manufacturability stems from the fact that the current running in the channel of the readout transistor is composed of similar type charges than the signal charges situated in the MIG modulating the current of the readout transistor. This arrangement can be realized by placing a potential barrier formed of fully depleted semiconductor material in between the channel and the MIG. The advantage is that the location of lowest potential energy for signal charges in MIG is well aligned with the location of lowest channel threshold.

The potential barrier between the channel and the MIG prevents also the mixing of signal charges with interface-generated charges meaning that a MIG sensor does not suffer from interface generated dark noise. Similarly this potential barrier separates also the signal charges from the interface during signal charge transfer (transfer is required for NDCDSR). Thus the MIG image sensor is not prone to image lag. Besides the potential barrier acts also as the vertical anti-blooming mechanism, i.e., when the MIG starts to be full of signal charges the excess charges will flow over the potential barrier preventing the signal charges from spreading into neighboring pixels.

The low 1/f noise is due to the fact that a deep buried channel can be utilized in a MIG sensor since non-circular readout transistor design is enabled. Besides the deeper the buried channel the bigger the signal and the smaller the signal the smaller the 1/f noise. The latter fact is because the less there is charge in the MIG the deeper the buried channel.

The good QE for NIR and visible light, the 100 % fill-factor, as well as low crosstalk are due to the thick fully depleted BSI design. Another reason for the low crosstalk is the fact that current mode readout is enabled. The reason why very fast readout is enabled stems from the current mode readout operation. The NDCDSR is due to the fact that it is possible to transfer the signal charges into and out of the MIG without destroying the signal charges. The fact that a MIG sensor has NDCDSR means that there is no accumulation of read noise, i.e. one can simultaneously obtain deep space images and track asteroids by utilizing a relatively high frame rate.

The fact that the MIG sensors do not suffer from interface problems (no interface generated dark noise, very low level of interface generated 1/f noise, no image lag) means that the MIG sensors are inherently radiation tolerant and suite thus well for space applications. The lack of interface problems has also the additional benefit that it enables low noise image sensors to be made from other semiconductor materials than silicon, which is not really possible with other image sensor technologies.

## II. DOUBLE MODIFIED INTERNAL GATE FIELD EFFECT TRANSISTOR DETECTOR

The investigated pixel structure is a thick fully depleted BSI deep buried channel double MIGFET pixel, wherein the signal charge can be transferred back and forth between the two MIGs of the pixel. Both MIGFETs have a buried internal gate (MIG) implanted directly underneath their conducting channels.

As can be seen from the cross-section on Fig.2 Source (S1), Gate1, Drain (D1) and MIG1 belong to the first MIGFET and Source (S2), Gate2, Drain (D2) and MIG2 belong to the second MIGFET. Between these two MIGFETs there is a Transfer Gate enabling transfer of the stored signal charge between two MIGs, which is necessary for the NDCDSR. One or preferably both nodes S1 and S2 are connected on separate vertical lines, which are connected to separate CDS readout circuitries. The D1 and D2 can be both connected to the same vertical line or to a node, which is common to the whole pixel matrix.

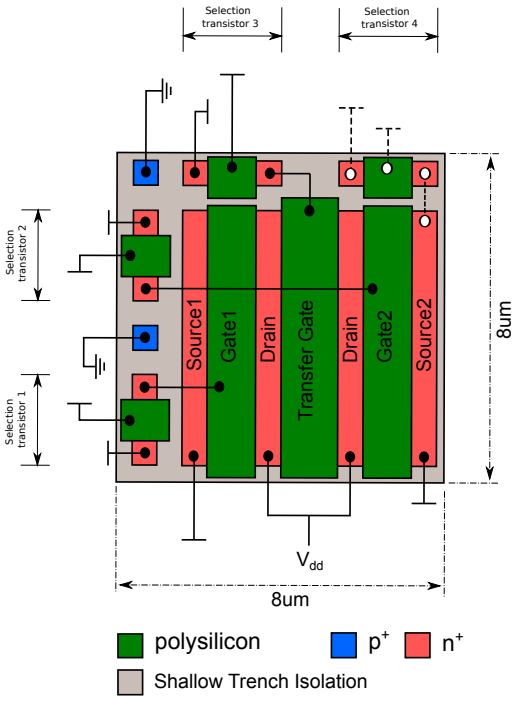


**Fig. 1.** Front side view of the Double Modified Internal Gate Field Effect Transistor Detector.

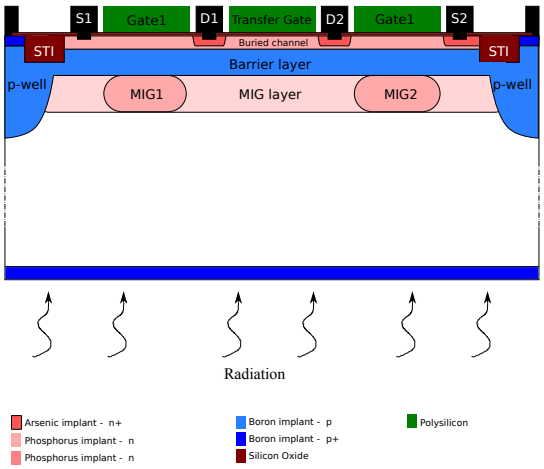


**Fig. 2.** Cross-section of the Double Modified Internal Gate Field Effect Transistor Detector.

The Gate1, Gate2, and Transfer Gate nodes are connected to separate horizontal lines.

The pixel comprises a 50 μm thick fully depleted $n^-$ type BSI silicon substrate and has dimensions of 8 by 8 μm. The front side of the device is manufactured utilizing a 0.18 um or smaller minimum line width 5 V CMOS process. The only change that is required to the CMOS process is to adjust it to the lower substrate doping of high resistivity wafers. The thinning of the wafer can be performed with TAIKO (a wafer back grinding process that uses a grinding method developed by DISCO) process [6] after which backside implant, laser annealing, and chip sawing may be performed.

The upper part of the pixel (i.e. front side) comprises a stack of an n-type buried channel implant, a p-type barrier implant acting as a barrier between the buried channel and the MIG layer, and a MIG layer. It also has a Shallow Trench Isolation (STI) and a p-well surrounding the pixel. The p-well reduces effectively cross-talk and prevents blooming. Besides one can place n type selection transistors into the p well in order e.g. to enable pixel specific reset. There are additional n-type implants in the MIG layer beneath Gate1 and Gate2 referred to as MIG1 and MIG2 and used for storing of signal electrons.

In this design the p well is held always at 0 V, the D1 and D2 always at +5 V, the S1 and S2 always at +4.5 V. The operational range of the nodes Gate1, Gate2, and Transfer Gate is from 0 V to +5 V.

## III. FULL 3D TCAD SIMULATION STUDY

The performance of the pixel has been studied by simulating operational steps. The first step is reset of the pixel, when all the charge present in the pixel is removed. The second step is integration, when charge accumulates in the MIGs. The third and fourth steps are Transfer and Measurement, when the charge is transferred from one MIG to another and non-destructive read-out is performed. In this paper we present simulation results for the pixel at -40°C.

### A. *Reset*

At first pixel reset operation is performed in order to remove any charge form the MIGs. The charge is removed into the nodes D1 and D2 by applying a reset potential configuration wherein the transfer gate is at +4 V (+4.5 V or +5 V could be equally well used) and nodes Gate1 and Gate2 are at 0 V. A two dimensional (2D) cross-section of the electrostatic potential distribution of the three dimensional (3D) simulation of the pixel in the reset potential configuration is shown in Fig. 3. Fig. 5 represents the electron density distribution on the same cross-section. Electrostatic potential distribution on the vertical cut-lines A, B, and C indicated in Fig. 3 are presented in Fig. 4. The 3D simulation results are obtained using the (Synopsys) TCAD software tool.

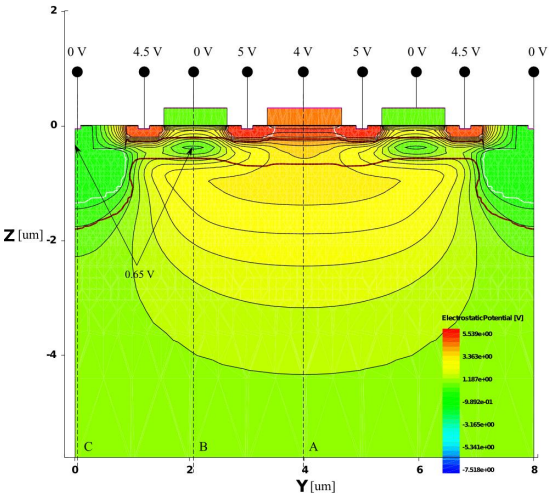


**Fig. 3.** Electrostatic potential distribution during reset on a 2D cross-section of a 3D simulation of the pixel structure. The potential curves on vertical cut lines A, B, and C are depicted on Fig. 4.

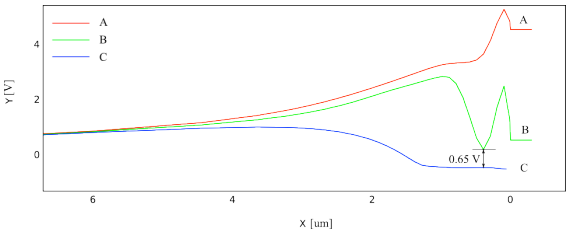


**Fig. 4.** Electrostatic potential during reset on vertical cut-lines A, B, and C depicted on Fig. 3. No interface leakage current from the depleted gate oxide interface can enter into the MIG since there is a potential barrier between the channel and the MIG as can be seen from curve B.

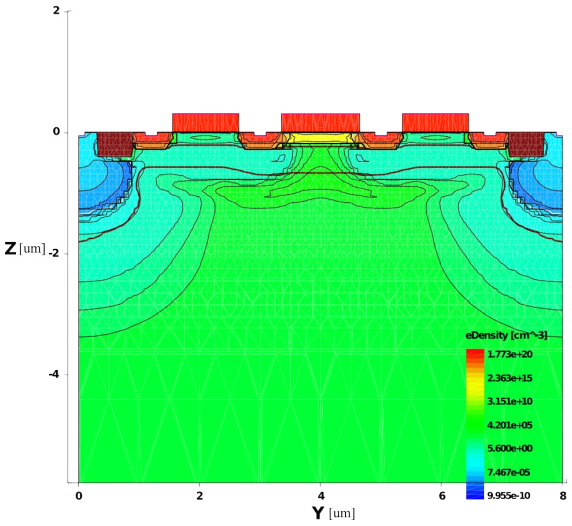


**Fig. 5.** Electron density distribution during reset on a 2D cross-section of the 3D simulated pixel. There is no charge left in the MIGs.

One can immediately deduce from Fig. 3 that during reset there is no electrostatic potential barrier from the two MIGs towards the drain contact and thus complete and very fast reset is enabled. One can also deduce from Fig. 3 that there is always a potential barrier for electrons that prevents electrons located at the interface or in the source, drain, or channel to enter into the MIG layer or into the MIGs. This can be also deduced from the electrostatic potential distributions on cut-lines A and B presented in Fig. 4.

B. *Integration*

The reset of the pixel is followed by an integration period wherein the nodes Gate1 and Gate2 are simultaneously biased at 1.5V and Transfer Gate is biased at 0V (or alternatively at a slightly higher potential like e.g. +1 V). The biasing of Gate1 and Gate2 nodes during integration is such that the channels underneath the gates are closed, i.e., the corresponding pixel row is not selected for readout.

In Fig. 6 the electrostatic potential distribution and in Fig. 8 the electron current distribution on a cross-section of the pixel is depicted at the end of the integration period. At this point 964 electrons are collected into the two MIGs (482 electrons in each MIG); the potential barrier from the MIG towards the drain contact is 0.74V and the potential barrier in between the MIGs is 0.58 V.

It can be deduced both from Figs 6, 7, and 8 that the interface generated electrons are effectively prevented from entering into the MIGs and MIG layer. It can be also seen from Fig.7 that there is a sufficient barrier between two pixels meaning that vertical anti-blooming mechanism is enabled.

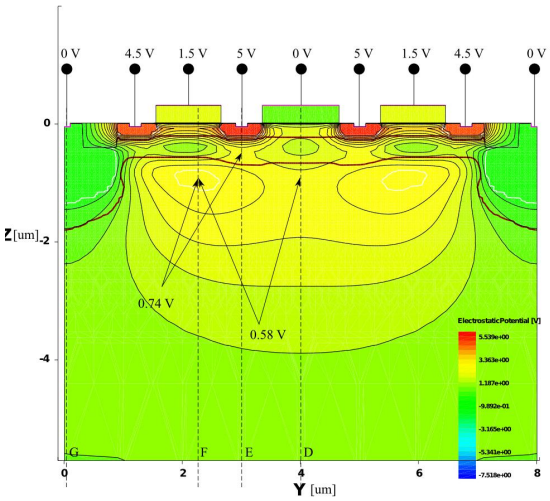


**Fig. 6.** Electrostatic potential distribution during integration on a 2D cross-section of the 3D simulated pixel when 964 electrons are located in the two MIGs (482 electrons in each MIG); the potential barrier from the MIG towards the drain is 0.74 V. The potential barrier between two MIGs is 0.58 V. The potential curves on vertical cut lines D, E, F, and G are depicted on Fig. 7.

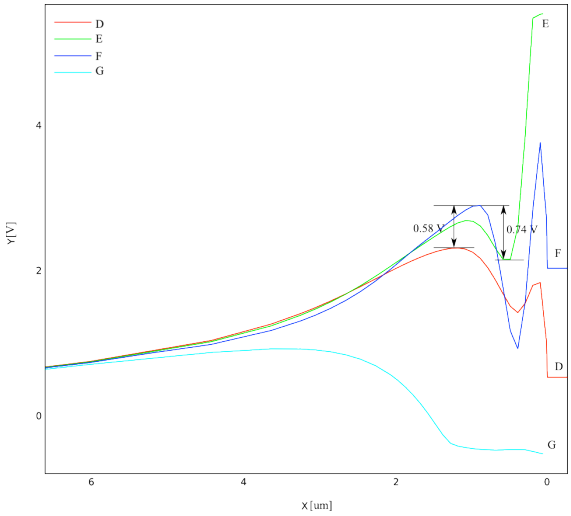


**Fig. 7.** Electrostatic potential during integration on vertical cut-lines D, E, F, and G depicted on Fig. 6. The signal charges in the MIG have a much smaller barrier (0.74 V) towards the drain than towards neighboring pixels (potential maximum of G subtracted from the local potential maximum of F at the depth of around 1 um). This means that vertical anti-blooming mechanism is enabled (excess signal charges flow into the drain and not to neighboring pixels).

C. *Basic CDS measurement procedure*

After the integration period and in the beginning of the read-out period a read-out potential configuration is first applied to the pixel wherein the nodes Gate1 and Gate2 are at +3.5 V and the Transfer Gate is at 0 V. At this stage one can

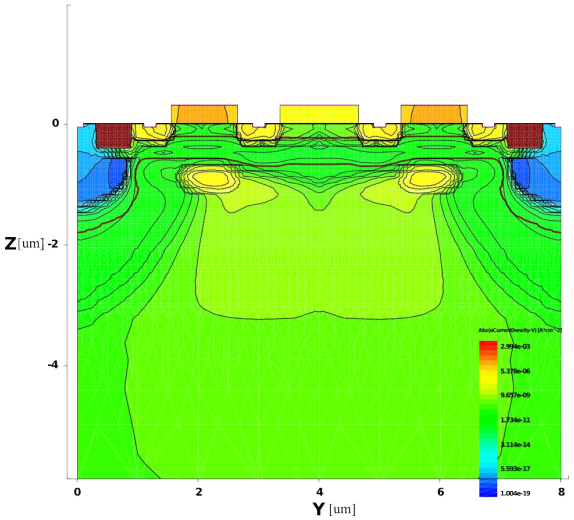


**Fig. 8.** Electron current distribution during integration on a 2D cross-section of the 3D simulated pixel when 964 electrons are located in the two MIGs (482 electrons in each MIG). The interface leakage current is effectively prevented from entering into the MIG layer.

already measure with the first or second or both MIGFETs whether the pixel is in saturation and if so one could use the logarithmic dependence of the readout result to expand the dynamic range. The preferable way for readout in the proposed pixel is source current mode readout [5] wherein the value of the electric current of the source current is measured when all nodes of the pixel being at fixed potentials as depicted in Fig. 11.

Next a charge transfer procedure is applied to the pixel wherein 0 V is first applied to the Gate2. Then the Transfer Gate is set to +2.5 V – this potential configuration is referred to as the transfer stage which is depicted in Fig. 9. Then the Transfer Gate is quickly set back to 0 V, and finally the Gate2 is brought back to +3.5 V. At this stage the pixel is back to the readout potential configuration and all the 964 signal charge electrons are located in MIG1 as depicted on Fig. 10.

One can now perform the first part of the CDS procedure for the second MIGFET (located on the right hand side) by storing the readout result of the second MIGFET. Next the Gate1 is brought to 0 V, then +2.5 V is applied to the Transfer Gate, after which the Transfer Gate is brought back to 0 V, and finally the Gate1 is brought back to +3.5 V. The pixel is now back at the measurement stage but all 964 signal charge electrons are located in MIG2.

At this stage one can perform the second part of the CDS procedure for the second MIGFET by storing the readout result of the second MIGFET. The final CDS readout result for the second MIGFET is obtained by subtracting the first readout result from the second one (or vice versa). In our case it is 41.9 μA – 4.05 μA = 1.34 μA. The charge to current conversion gain is obtained by dividing 1.34 μA by 964 electrons resulting in 1.4 nA/e. It is important to note that during the CDS readout process of the second MIGFET all the potentials on the nodes of the second MIGFET remained fixed.

If desired one can perform during the second part of the CDS procedure for the second MIGFET also the first part of the CDS procedure for the first MIGFET by storing the readout result of the first MIGFET. Then the Gate2 is brought to 0 V, next the Transfer Gate is set to +2.5 V after which it is brought back to 0 V, and then the Gate2 is brought back to +3.5 V after which one can perform the second part of the CDS procedure for the first MIGFET by storing the readout result of the first MIGFET. The final CDS readout result for the first MIGFET is obtained by subtracting the first readout result from the second one.

If desired one can perform during the second part of the CDS procedure for the first MIGFET again the first part of the CDS procedure for the second MIGFET. In other words one could sequentially perform as many CDS measurements as desired with both of the MIGFETs.

From the electrostatic potential distribution presented in Fig. 9 one see that during the transfer stage there is no potential barrier from the energetically non-preferable MIG towards the energetically preferable MIG. The potential barrier from the energetically preferable MIG towards the drain contact is 0.5 V. The electron density distribution during the charge transfer potential configuration is presented in Fig. 9 from which it can be deduced that all the 964 electrons are successfully transferred to the left MIG.

The electrostatic potential distribution during the measurement potential configuration when the 964 electrons are in the left hand side MIG is depicted in Fig. 11.

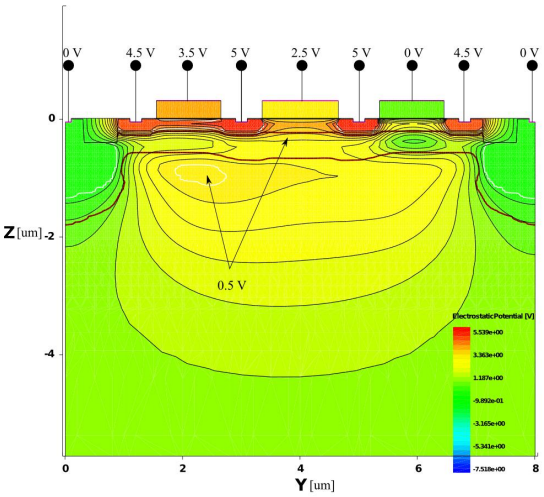


**Fig. 9.** Electrostatic potential distribution in charge transfer potential configuration on a 2D cross-section of the 3D simulated pixel after signal charge electrons have been transferred to the left MIG.

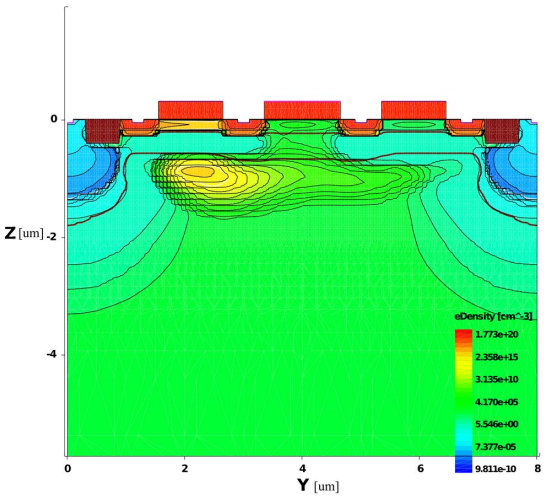


**Fig. 10.** Electron density distribution in charge transfer configuration on a 2D cross-section of the 3D simulated pixel after signal charge electrons have been transferred to the left MIG.

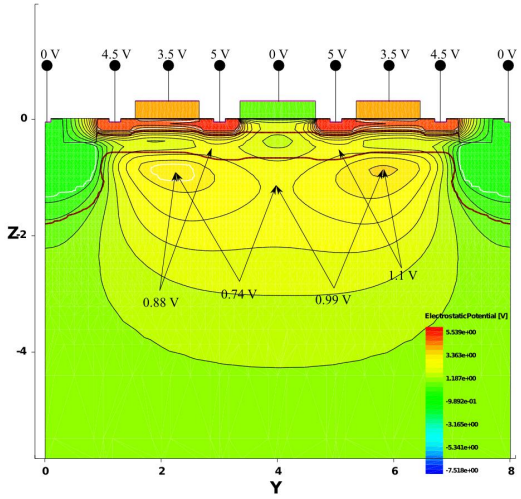


**Fig. 11.** Electrostatic potential distribution in the measurement potential configuration on a 2D cross-section of the 3D simulated pixel. The barrier from the MIG containing 964 electrons to the empty MIG is 0.74 V. The barrier from the MIG containing 964 electrons to the drain is 0.88 V. The barrier from the empty MIG to the full MIG is 0.99 V. The barrier from the empty MIG towards the drain is 1.1 V.

The minimum potential barrier from the MIG having 964 electrons towards the drain contact is 0.88 V and the potential barrier from the MIG having 964 electrons to an empty MIG is 0.74 V.

D. *Other operation schemes*

It should be noted that the proposed pixel architecture is very basic one and that many other designs could be utilized. Beside the basic operation scheme already presented there are also many others. One could for instance utilize the charge transfer stage also as integration stage by connecting the drain of a selection transistor to the source of the MIGFET, which MIG is used for the collection of the signal charges. This could improve the accuracy of the logarithmic readout.

In case of the transfer stage is utilized also as the integration stage one could initiate the readout stage by opening the selection transistor for the source node and perform an initial measurement. If the pixel would be already in saturation one could utilize pixel specific reset for the pixel, come back to the transfer stage and perform yet another measurement. Then in between actual NDCDS measurements (see chapter C) one could perform a readout during every transfer stage with the MIGFET to which MIG the signal charge is being transferred. Such readout results would enable in the linear readout region a fast and easy way to monitor the buildup of signal charge during the readout period. In this manner the dynamic range of the linear region could be improved considerably.

In case of pixel specific reset the pixel is reset only if amount of signal charges in the pixel approaches saturation (e.g. if the amount of signal charge equals or is larger than 50 % of the saturation value). The pixel specific reset can be easily accomplished by connecting one gate and the transfer gate to drains of selection transistors and by connecting the gates of the selection transistors vertically to a reset selection circuitry. One could also connect the remaining gate vertically to the reset selection circuitry in order obtain broader control of the pixel.

It is also possible to increase the dynamic range by utilizing one short and one long integration time per frame [7] and preferably so in conjunction with pixel specific reset [8]. If the separation of the two rows being subsequently readout is small then a very short integration time is enabled in conjunction with pixel specific reset. The pixel specific reset enables on the other hand a very long integration time lasting several frames. For these reasons high dynamic range is enabled.

Yet another way to improve the dynamic range is to divide the matrix in stripes containing preferably equal amount of rows and to utilize individual readout circuitries for each stripe. In this manner rows in different stripes can be readout simultaneously. This solution increases naturally the amount of circuitry on the chip and the amount of vertical source lines running across the pixel matrix. The latter one is not problematic from crosstalk point of view due to current mode readout since the potential of the source lines remains fixed.

It is also possible to divide the pixel matrix into odd and even lines having separate readout, horizontal selection, and vertical selection circuitries as well as separate vertical source lines. In this manner one short and one long integration times

during one frame could be utilized without reducing the frame rate.

## IV. CONCLUSIONS

The 8 um pitch double MIG pixel structure designed for a slightly modified 0.18 μm or smaller line width 5 V CMOS process was presented and simulated in 3D. On the basis of this study, it can be effectively used in radiation hard imaging applications and the reason is that the pixel does not suffer from interface issues (i.e. there is no interface generated dark noise, no interface generated image lag, and virtually no interface generated 1/f noise).

The reason for the lack of interface generated dark noise and image lag is due to the fact that in the simulated MIG pixel structure there is always a big enough potential barrier in between the signal charges and the depleted interfaces. The very low interface generated 1/f noise stems from the deep buried channel – the potential difference from the bottom of the buried channel to the interface is 0.45 V to 0.68 V throughout the length of the buried channel.

Furthermore the 50 um thick fully depleted BSI pixel design offers several advantages like 100% fill factor, high QE for NIR and visible light, low crosstalk, anti-blooming, and very high readout speed. The last mentioned fact is due to the current mode readout as well as due to the fact that in reset and charge transfer stages there are no potential barriers hindering the signal charge transport.

The anti-blooming is due to the fact that the potential barrier for signal charges situated in MIG is always much lower towards the drain than towards the neighboring pixels as can be seen from the cut-lines D, E, F, and G in Fig. 7. At measurement and transfer potential configuration the signal charges are located underneath the gate biased at higher positive voltage than during integration and thus the anti-blooming protection is even better during other modes than during integration.

From the above results one can see that the transfer stage limits the Non-Destructive Correlated Double Sampling Full Well Capacity (NDCDSFWC) of the pixel, i.e., the maximum amount of signal charge that can be successfully stored, readout, and transferred from one MIG to another. The reason for this is that the barrier for signal charges located in the MIG to escape to drain or to an empty MIG is by far the smallest during the transfer stage. At the level of 964 signal electrons no charge loss was identified. The NDCDSFWC is estimated to be somewhere in between 1000 and 2000 electrons at -40$^{o}$C.

According to the 3D simulations the Charge Conversion Gain for 964 electrons at -40° Celsius is 1.4 nA per signal electron.

According to the simulations the thick fully depleted backside illuminated pixel design posses considerably more favorable properties for space applications than a previously simulated thin front side illuminated double MIG pixel structure [9].

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