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LOW NOISE WDR ROIC FOR INGAAS SWIR IMAGE SENSOR

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INTRODUCTION

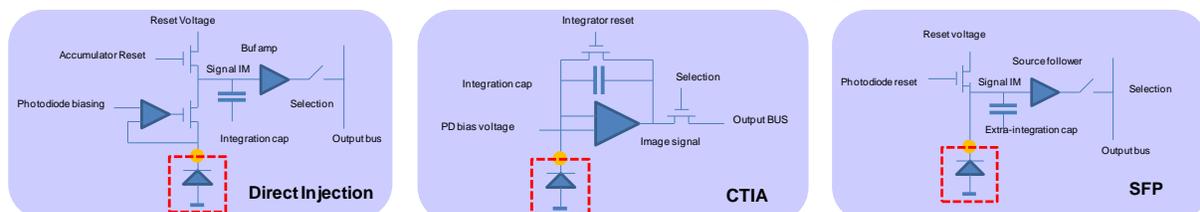
Hybridized image sensors are actually the only solution for image sensing beyond the spectral response of silicon devices. By hybridization, we can combine the best sensing material and photo-detector design with high performance CMOS readout circuitry. In the infrared band, we are facing typically 2 configurations: high background situation and low background situation. The performance of high background sensors are conditioned mainly by the integration capacity in each pixel which is the case for mid-wave and long-wave infrared detectors. For low background situation, the detector's performance is mainly limited by the pixel's noise performance which is conditioned by dark signal and readout noise. In the case of reflection based imaging condition, the pixel's dynamic range is also an important parameter. This is the case for SWIR band imaging. We are particularly interested by InGaAs based SWIR image sensors.

Currently the CMOS readout circuits are mainly based on active charge accumulation methods (direct injection, CTIA and source-follower-per-pixel). Even with continuous effort of ROIC design community, the readout noise ($\sim 40e$) [1][2] remains very high compared to CMOS active pixel design [3] ($< 1e$), even with a very high conversion factor by sacrificing the pixel dynamic range in the design. The main reason for this limitation is the impossibility of high speed CDS (correlated double sampling) inside the pixel. As will be discussed in next sections, the CDS interval in actual ROIC design is made on the integration period which can be as long as tens of millisecond in video rate and even longer in slow integration case. When sub-micron CMOS process is used for fine pitch ROIC design, the higher $1/f$ noise in CMOS devices becomes even more limiting. In this presentation, we present a new charge sensing concept for InGaAs SWIR sensors. This readout circuit structure can give potentially single electron readout noise performance. In the following sections, we will at first present 3 conventional ROIC designs and also NIT's wide dynamic range solar-cell mode logarithmic ROIC design. Then we will introduce the new charge injection and transfer based low noise ROIC design concept which could give ultra-low noise linear response and a wide dynamic range logarithmic response at the same time.

Conventional ROIC element designs

Conventional ROICs (Read Out Integrated Circuits) use one of the 3 sensing elementary circuits: Direct Injection (DI), Capacitive Trans-Impedance Amplifier (CTIA) and Source Follower per Pixel (SFP) as shown in Fig. 1.

Figure 1. 3 conventional ROIC elementary designs.



Most of the low noise designs use CTIA based structure. The fundamental reason is that the high voltage gain of the trans-impedance amplifier can attenuate the low frequency noise by the capacitive feedback loop. The photo-detector's bias voltage is clamped by the virtual ground made by the op-amp, so low biasing voltage can be used for a lower dark current in the detector. In a simple design, the offset voltage of the op-amp will limit the lowest bias voltage applied on the detector element. [4] proposed auto-zeroing on the op-amp in order to be able to use zero-bias for the detector element. In this case, the RMS noise of the dark current will be increased by 3dB but a long exposure time can be used without saturating the integration capacitor by the dark current. The reference [5] gives a very good review of ROIC designs.

NIT's Solar-cell mode logarithmic ROIC design

As stated in the introduction, in reflection based imaging conditions, the dynamic range (DR) of detector is of great importance. Increasing DR by using larger integration capacitor is not always possible either due to large readout noise or due to the limitation of pixel pitch. One of the solutions is to use non-linear photo-electric response. The logarithmic response is considered as the most interesting one for the following reasons: 1) very wide DR thanks to logarithmic compression; 2) contrast response independence from scene illumination; 3) easy implementation thanks to many exponential phenomena in electronic circuits and device physics. Conventional logarithmic pixel designs use the exponential current-voltage relationship in a sub-threshold MOS transistor. This sub-threshold MOS transistor transforms the linear photocurrent coming from the photo-detector into a logarithmic voltage as image signal. The drawbacks of this approach are numerous: 1) high fixed pattern noise due to the conversion MOS transistor; 2) low sensitivity due to the leakage current in the MOS transistor; 3) image lag due to the absence of reset possibility and 4) loss of sensitivity with temperature since the high dark current will wash out rapidly the image contrast even at moderate temperature.

The approach used in NIT's InGaAs logarithmic sensors use the photo-detector as a solar-cell of which the open-circuit voltage is sampled as image signal [6]. This simple arrangement gives a breakthrough improvement compared to conventional logarithmic design: 1) FPN can be suppressed by reading a zero voltage on the photodiode which is created by a MOS transistor; 2) sensitivity is improved since no leaky element is put with the photodiode; 3) the reset MOS suppressed the image lag. Fig. 2 illustrates the basic structure of NIT solar-cell mode ROIC pixel design.

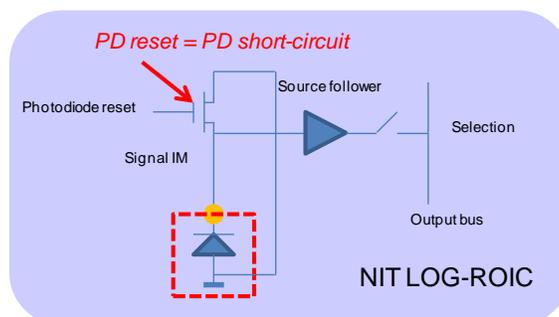
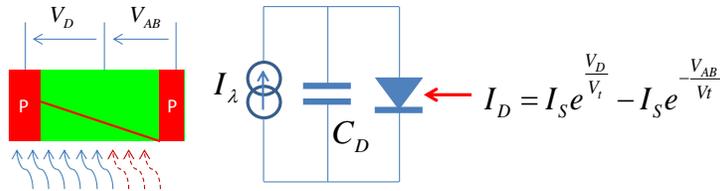


Figure 2. NIT solar-cell mode ROIC pixel structure. It should be noted that the source follower can be replaced by a voltage amplifier too.

In NIT's approach, we use special InGaAs photodiode array design which incorporates lateral anti-blooming structure inside the pixel array. The solar-cell mode photodiode can be modeled by the equivalent structure in Fig. 3.



Figur 3. Equivalent circuit model of solar-cell mode photodiode with lateral anti-blooming node.

By resolving the differential equation of the equivalent circuit in Fig. 3, we can get the complete response of the solar-cell mode photodiode as:

$$V_D = V_T \ln \frac{I_\lambda + I_{AB}}{[(I_\lambda + I_{AB})e^{\frac{V_{D0}}{V_T}} - I_s]e^{\frac{(I_\lambda + I_{AB})t}{V_T C_D}} + I_s} \quad \text{where } I_{AB} = I_s e^{\frac{V_{AB}}{V_T}}$$

We can plot the response curve under different temperatures by increasing the junction saturation current as shown by Fig. 4. It should be noted that the temperature effect in this case appears as a simple level shift of the photoelectric response which is very easy to compensate but the logarithmic response is conserved even at very high temperature.

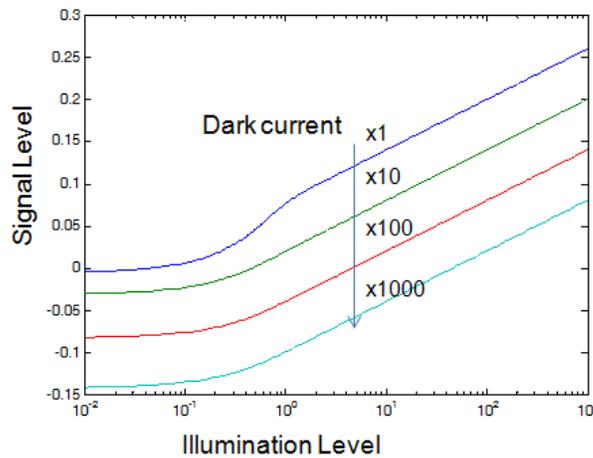


Figure 4. The voltage response of the solar-cell mode photodiode with lateral anti-blooming node (arbitrary units are used here.).

We have developed several InGaAs SWIR sensors by using this patented concept and structures and have demonstrated excellent image quality without any active cooling and temperature stabilization of the sensor. The dynamic range of these sensors exceeds 120dB without any special processing and the camera electronics has been simplified to a minimal level. But the drawbacks of this approach are: 1) high sensing node capacitance resulting in a very low conversion factor and 2) absence of CDS due to the absence of charge conservation in a solar-cell mode photodiode. Both of these drawbacks raise the readout noise level of the sensor which is about hundreds of electrons.

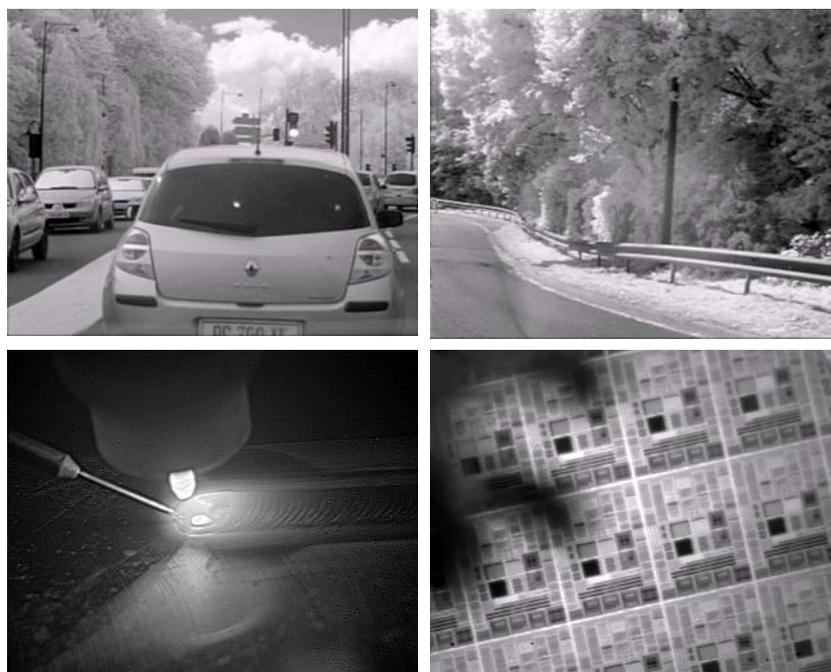


Figure 5. Some example images captured by NIT Solarcell mode InGaAs sensors. Please note the extremely high dynamic range of the arc welding scene.

NIT's Charge-Injection-Accumulation-Transfer (CIAT) ROIC element design

The rapid progress in CMOS active pixel sensor is mainly related to charge transfer pixel design associated with fully depleted pinned photodiode. This association of fully depleted pinned photodiode and charge transfer is actually the best configuration for low noise photon detection: 1) fully depleted pinned photodiode suppresses the KTC noise and reduces considerably the surface dark current ; 2) charge transfer permits the use of low capacitance sensing node with high conversion factor in order to lower the downstream noise and 3) finally the charge transfer permits pixel-wise duration CDS operation with a maximum $1/f$ noise suppression efficiency. We would like to introduce this approach in ROIC design in order to get the lowest readout noise.

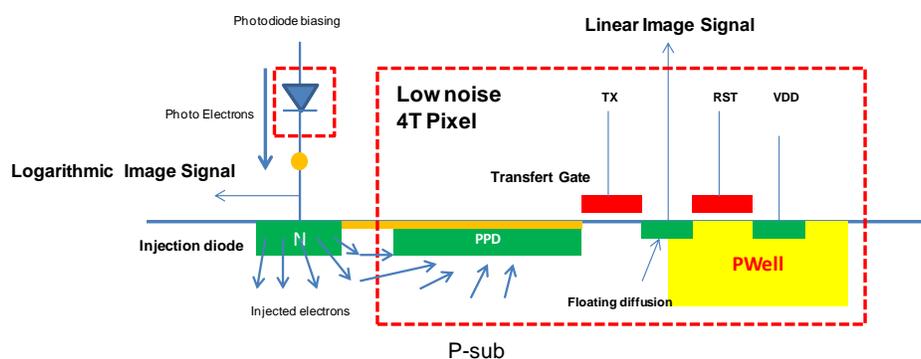


Figure 5. The Injection-Accumulation-Transfer (IAT) ROIC element proposed by NIT.

The new concept patented by NIT is shown in Fig. 5 where the photo-generated charge is electron. An injection diode is placed close to a traditional 4T CMOS active pixel. This injection diode is connected through the flip-chip contact to an external photodiode. The collected photo-charge from the external photodiode is injected into the substrate via this injection diode and then collected by the pinned photodiode in the 4T pixel.

The pinned photodiode is fully depleted at the beginning of the integration and its charge is transferred to the floating diffusion at the end of the integration. The voltage change on the floating diffusion due to the arrival of the collected photo-charge gives the image signal. A CDS will be used to remove the KTC noise on the floating diffusion. Fig. 6 gives the operation timing diagram of this ROIC element for the linear response.

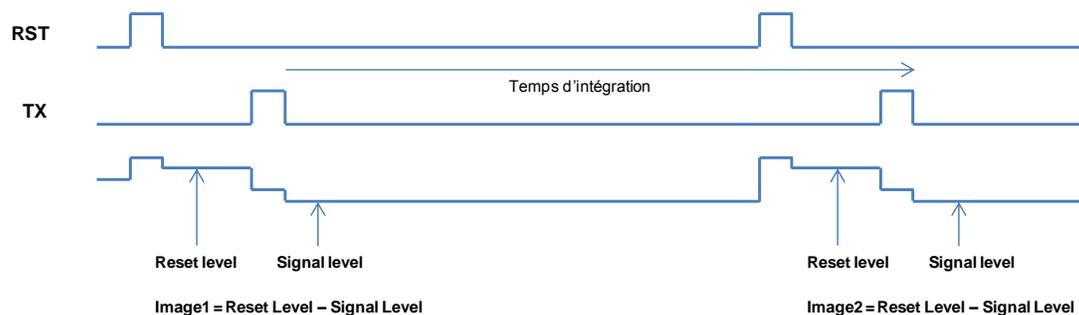


Figure 6. The timing diagram of the ROIC element in Fig. 5. The image signal generated here corresponds to the linear response of the ROIC element.

From Fig. 5, it can be noted that the voltage of the injection diode can be also read and this voltage gives a logarithmic response, almost the same as the one from Fig. 3. The pinned photodiode here plays the anti-blooming node in fact. Special process engineering is needed in order to maximize the charge injection and collection efficiency. Engineering recipes used in BJT can be largely used for this purpose.

In order to implement IAT approach in a standard CMOS process, we have developed/patented a new pinned photodiode and charge transfer structure. This structure can be virtually implemented in all CMOS process by adding some dedicated ion implant steps which precedes CMOS transistor formation in order to keep constant thermal budget for CMOS devices. This process has been tested on a small 4T pixel array (320x240) of 10um size with success. The readout noise has been measured at 6 electrons (including dark current contribution). The only issue is that the dark current, measured at about 100pA/cm², is still too high for low light imaging. But for SWIR InGaAs sensor, this dark current is at least 20X lower and it should be acceptable for ROIC applications. Fig. 7 shows some captured images and also RMS noise distribution in dark. This achievement permits a full design freedom in ROIC development since 4T process provided by most of CMOS foundries has very limited design freedom. A prototype InGaAs sensor with this readout element is under development at NIT.

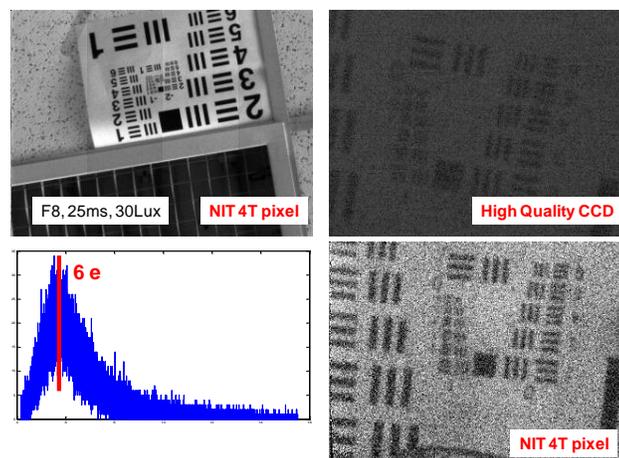


Figure 7. Captured images from the 4T test chip and the measured RMS noise distribution histogram.

Conclusion

In this paper, we have presented the ROIC element concepts and technologies developed at NIT. We have presented in some details the unique solar-cell mode photodiode logarithmic InGaAs sensors and shown that this new logarithmic pixel design suppress most of the shortcomings in the conventional logarithmic pixel structure. The main contribution of this paper is the introduction of Charge-Injection-Accumulation-Transfer (CIAT) pixel design which can give potentially sub-electron readout noise and a wide dynamic range logarithmic response at the same time by the same pixel. We are working on the development of such a sensor with InGaAs material.

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