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MiniDSS: A low-power and high-precision miniaturized digital sun sensor

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Abstract— A high-precision and low-power miniaturized digital sun sensor has been developed at TNO. The single-chip sun sensor comprises an application specific integrated circuit (ASIC) on which an active pixel sensor (APS), read-out and processing circuitry as well as communication circuitry are combined. The design was optimized for low recurrent cost. The sensor is albedo insensitive and the prototype combines an accuracy in the order of 0.03° with a mass of just 72 g and a power consumption of only 65 mW.

Keywords- Sun sensor; DSS; Active Pixel Sensor; AOCs sensor

I. INTRODUCTION

A prototype of a low-power and high-precision miniaturized digital sun sensor (miniDSS) was developed at TNO. High-precision sun angle measurement has conventionally been associated with costly, bulky and power hungry devices [1, 2]. Contrary, the miniDSS, which is shown in Figure 1, provides a cost-effective, miniaturized and low-power alternative, while maintaining comparably high accuracy.



Figure 1: Photograph of the miniDSS prototype.

The miniDSS prototype is fully functional and is expected to be launched on QuadSat in 2012 for in-orbit demonstration. This satellite program is a cooperation between Angstrom Aerospace Corporation (Sweden) and OHB (Germany) and is designed to demonstrate the potential of Plug and Play interface technology. Further development towards qualified

models is planned in close cooperation between TNO and Moog Bradford (formerly known as Bradford Engineering). Moog Bradford has already a long working relationship with TNO and produces large quantities of analogue sun sensors based on TNO designs.

II. OPERATION

The heart of the system is an advanced active pixel sensor (APS) as detector behind a pinhole sized aperture, through which sun light penetrates and incidences on the pixel array.

The principle of operation is shown in Figure 2 and is based on the precise measurement of the location of the centre of luminosity of sunlight projected onto the APS.

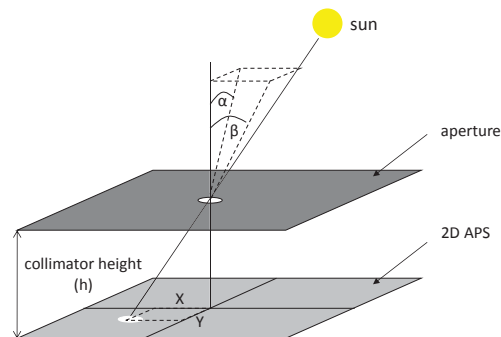


Figure 2: Operation principle of the miniDSS.

The location of the centre of the sun spot is provided to the space craft (S/C) in the form of an X and Y value from which the sun aspect angles α and β are easily calculated. The relation between Y and sun aspect angle α is given by

$$\alpha = \arctan\left(Y \cdot \frac{s}{h}\right), \quad (1)$$

in which Y is the distance in pixels along the y -axis between the centre of the APS and the centre of the sun spot, s is the pixel size and h is the collimator height, i.e. the distance

TNO gratefully acknowledges the financial support of the Dutch micro-technology development program MICRONED for the development of the APS+ and the Netherlands Space Office (NSO) for their financial support of the design and development of the sensor core and the housing.)

between the aperture and the APS. Sun aspect angle β is calculated in similar fashion, i.e.

$$\beta = \arctan\left(X \cdot \frac{s}{h}\right), \quad (2)$$

in which X is the distance in pixels along the x -axis between the centre of the APS and the centre of the sun spot.

In principle, no calibration look-up table (LUT) or temperature compensation is required to obtain a moderately high accuracy of the measured sun aspect angles. Small unit-specific deviations from the desired aperture position in the x , y and z direction, with respect to the pixel array are easily obtained from a very limited calibration procedure. In order to achieve a high accuracy, these misalignments can be compensated for by adding the misalignment values to X , Y and h , respectively. Without taking these numbers into account the accuracy is still in the order of 0.3° . In cases where such an accuracy is sufficient, a unit level calibration may be omitted, significantly reducing the recurrent cost of the sensor.

The miniDSS has two operating modes. Upon power-up the miniDSS starts in the acquisition mode, in which presence and coarse location of the sun spot on the pixel array are determined. At detected sun presence, the miniDSS transitions into the tracking mode in which a region-of-interest (ROI) of 25×25 pixels around the coarse location is read-out with high accuracy to determine the center of the sun spot. If sun presence is lost, the miniDSS transitions back into the acquisition mode.

A. Acquisition mode

The miniDSS starts working in an acquisition mode. The purpose of the acquisition mode is to decide a 25×25 pixel region-of-interest (ROI) which contains the complete sun spot (10×10 pixels). Typically, the pixel array is scanned from top left to top right and progressed line by line to the bottom right hand corner. However, in the miniDSS design this ROI is decided according to row and column profiling information of the pixel array. The profiling is achieved by a specific pixel design. The pixel array is surrounded by two addressing circuits: one for the Y or row addressing, the other one for the X or column addressing. By accessing all rows at once, the pixels on a single column are all "short-circuited" to the same read-out circuitry. The value that is read out is in that case dominated by the pixel with highest intensity within that column. I.e., if one of the pixels within that column is illuminated by the sun, the amplitude read out from that column will be high. The purpose is to find the columns with at least one pixel illuminated above a predefined threshold. In this way a profile of the columns with highest intensity can be obtained. A similar approach is used to find the rows comprising the pixels with highest amplitude. Hence, the combination of rows and columns with highest amplitude specify the ROI to use in the tracking mode. In order to avoid false sun spot detection as result of faulty, i.e. "always on" pixels, sun presence is only assumed if at least 3 adjacent columns and rows show amplitudes above the threshold. The

row and column profiling is schematically represented in Figure 3. Contrary to conventional digital sun sensors, as result of the employment of the profiling principle, acquisition and tracking modes are characterized by similar power consumption. Moreover, the miniDSS can locate the coarse sun position within the readout time for two lines. Therefore, compared to conventional digital sun sensors, the miniDSS is characterized by a much shorter acquisition time.

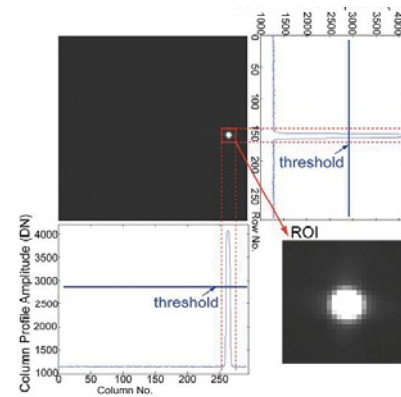


Figure 3: Schematic representation of the row and column profiling principle.

B. Tracking mode

Upon sun acquisition, the miniDSS transitions to the tracking mode in which only the 25×25 pixel ROI around the sun spot, commonly referred to as the tracking window, is read out. Using a centroiding algorithm, the center of the sun spot is accurately determined from the intensities registered by the pixels in the tracking window. The miniDSS periodically sends X and Y values with a precision of 15 bit to the S/C, representing the real-time sun-spot position. Using this precision, a sub-pixel resolution of $1/64$ pixel is achieved. I.e., 9 bits identify the pixel closest to the sunspot center and the 6 remaining bits convey the deviation of the exact location of the sun spot center from that nearest pixel.

In the vast majority of expected orbital positions, the tracking window will not be illuminated by earth albedo. However, in limited situations part of the tracking window (ROI) may be illuminated, affecting the accuracy of the centroid algorithm somewhat. Analysis has shown that the maximum angular error is $1.4 \cdot 10^{-3}^\circ$, as result of the earth albedo in worst case scenario. The miniDSS is therefore effectively albedo insensitive. This is considered a large advantage over analog sun sensors.

III. DESIGN

The miniDSS is designed as a low-power, low-volume, low-cost and low-mass sensor without compromising on accuracy. Figure 4 depicts a cross-section of the miniDSS design. The core of the miniDSS is the application-specific integrated circuit (ASIC) APS+. This chip is carried on a ceramic chip carrier, which furthermore carries peripheral electronics and a ceramic spacer. This spacer hold the sapphire aperture at a well-controlled distance above the APS+. The carrier is placed in an aluminum housing of which the top-

cover comprises a sapphire window, such that the sensor is exposed to direct sunlight.

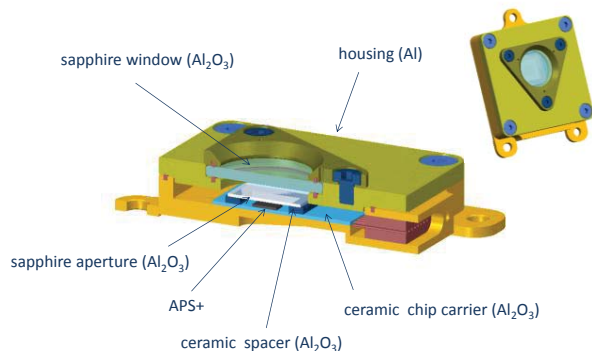


Figure 4: Cross-sectional view of the miniDSS design.

A. ASIC design

The miniDSS is a single-chip solution. The ASIC, which forms the core of the sun sensor and is shown in Figure 5. The APS+ not only comprises a 2D active pixel array, but also the read-out circuitry, a sequencer, the sun centroid algorithm and communication functionality. It was designed in a 0.18 micron CMOS process, which is characterized by low power consumption, high radiation tolerance and is furthermore cost effective. The ASIC measures only 5x5 mm².

The APS+ comprises 368x368 pixels with a pixel size of 6.5 μm. The individual pixels comprise only p-type transistors in order to minimize the probability of latch-up occurrence. This design choice results in a lower quantum efficiency (~25%) compared to pixel arrays employing both p-type and n-type transistors. However, this is not an issue given the large intensity of the sun light. Furthermore, abundant substrate contacts have been implemented to further reduce latch-up sensitivity.

The read-out circuitry consists of the necessary drivers for the pixel array, as well as a 10 bit pipelined analog-to-digital converter (ADC) to convert the pixel signals to the digital domain.

Switching from one mode to the other, control and timing within the various modes is managed by the sequencer.

The digital core furthermore comprises the centroiding algorithm, which determines the location of the sun spot, as well as the communication circuitry. Two mutually exclusive communication interfaces have been implemented: RS-422 (UART) and SPI.

The APS+ chip has a number of jumper inputs to externally control specific parameters. During assembly of the unit, the individual jumper inputs are wire-bonded to ground or left floating in order to set the parameters as desired. Default, the jumper inputs are high, as result of internal pull-up resistors. Parameters that can be set by these jumpers include the rate of data output (0.5, 1, 2 or 10 Hz), the initial integration time (and thus sensitivity) of the pixel array for both acquisition and tracking mode and the communication interface characteristics.

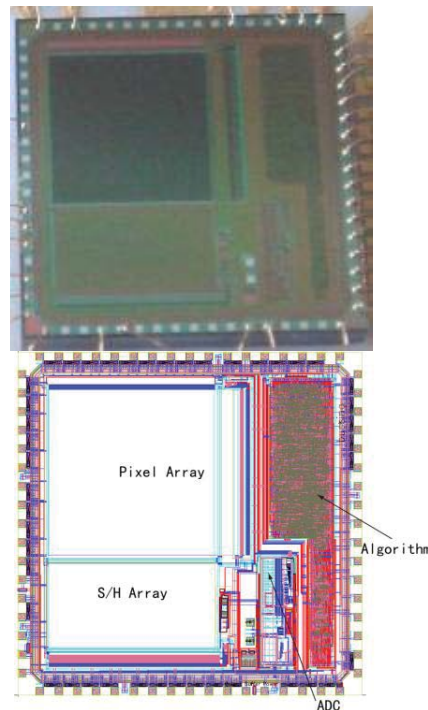


Figure 5: Photograph of the APS+ chip (top) and layout (bottom).

Several settings can be changes by telecommand (TC). For example, the integration time can be changed individually for acquisition mode and tracking mode. Furthermore, the field of view (FOV) can be set to four predefined values. Figure 6 depicts the area of the pixel array that is active for different settings for the fields of view parameter. As can be seen, the active size of the array can be reduced in steps of 1/4th of the original size. This is particularly useful if part of the S/C, e.g. a solar array, is in the FOV. In that case a smaller FOV can be chosen to prevent possible misidentification of the sun spot as result of direct reflection from the solar array.

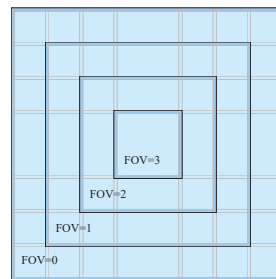


Figure 6: Parts of the pixel array active for the different user-selectable fields of view.

B. Housing design

The housing is machined from aluminum with alodine treated outer surfaces, instead of the more commonly used nickel iron alloy (Kovar) with gold plating. Aluminum has a lower density, is inherently non-magnetic, easier to obtain and

easier to machine. Moreover, aluminum has a good thermal conductivity, which is advantageous from a thermal point of view and the package material matches perfectly well with (small) S/C panels and brackets, which are typically made from aluminum as well. The alodine treated surfaces of the package provide a better interface for adhesion of the ceramic chip carrier and of the integrated connector.

An important feature for internal and external alignment of the sun sensor is the lay-out of the three mounting feet, which provide the mechanical interface of the miniDSS. They are coplanar and designed such that one foot has a calliper hole, which is also the mechanical reference point for the miniDSS, a second foot has a slotted hole and the third foot has a slightly oversized hole. By applying specific fasteners with calliper shafts, rotational alignment of the sensor can be assured. This provision is also used during the assembly of the APS+ chip to ensure alignment of the planar axes of the sensor, co-aligned with column and row directions of the image section of the APS+ chip, with the mounting feet. These provisions, in combination with the use of pick and place technologies for assembly of the APS+ chip in the housing, allow for low-cost production of units with high uniformity.

The optical interface of the housing consists of a 2 mm thick radiation tolerant sapphire window. The window is coated with an optical attenuation filter to avoid saturation of the APS+ image sensor. An Indium Tin Oxide (ITO) coating on top of the window ensures electrical conductivity for all external surfaces. This prevents the accumulation of static charge on the exterior of the window. Although sapphire can be welded into aluminum packages, it has been decided to clamp the window in the housing with conductive rubber seals on both sides, polymerized into the top-cover and triangular window clamp, respectively. This allows easy exchange of the optical window, e.g. for a window coated with a mission-specific attenuation filter.

The housing comprises an integrated custom connector. The company Axon (France) has developed a 13-pin hermetic single row nano-D connector which uses the same type of pins as used in their standard space micro-D products. This solution was chosen because the height of the unit is, for such miniaturized sensors, largely determined by the size of the connector. By using a custom integrated connector instead of a conventional micro-D connector, the height of the unit could be significantly reduced.

In order to obtain hermiticity, conductive seals are also employed between the part of the housing that holds the chip carrier and the top-cover. These seals are polymerized into the housing parts. The conductive seal material is ECSS compliant with regard to total mass loss (TML) and Collected Volatile Condensable Materials (CVCM).

C. Chip carrier design and aperture design

A ceramic chip carrier was produced by high-reliability hybrid manufacturer Lewicki GmbH (Germany). The chip carrier carries the bare APS+ die, the surface mounted device (SMD) peripheral electronics, and the spacer with aperture. The chip carrier is adhered to the housing using a thermally conductive ceramic filled silicon adhesive. This adhesive is characterized by good performance regarding thermal cycling of bonded materials with different coefficients of thermal

expansion (CTE), such as ceramic and aluminum. Figure 7 shows a photograph of the carrier with peripheral electronics in the housing, before assembly of the chip, spacer and aperture.

For the sensor core, materials with well-matched CTE were selected, to maximize the number of thermal cycles that the unit is able to withstand. For example, both the chip carrier and the spacer that is used to maintain a well-controlled distance (collimator height h) between the pixel array surface and the aperture are ceramic (Al_2O_3). Moreover, the aperture itself is made of sapphire (Al_2O_3), which is radiation tolerant. The coefficients of thermal expansion of these materials is in the order of $5 \cdot 10^{-6} / ^\circ\text{C}$, while that of the ASIC (Si) is $3 \cdot 10^{-6} / ^\circ\text{C}$.

The aperture consists of a metallization layer that is vacuum-deposited on the ceramic carrier. A pinhole of $65 \mu\text{m}$ in diameter is made in this metallization layer by a lift-off technique.

Chip, spacer and aperture are assembled using pick and place machinery in order to minimize misalignment. The alignment is performed with reference to the mechanical reference point.



Figure 7: Ceramic chip carrier carrying the SMD peripheral electronics.

D. Electrical interface

The supply voltage of the unit is 5 V, which is internally down-regulated to 3.3 V and 1.8 V required by the APS+ chip. Differential communication is performed at 0-3.3V levels, and the lines are driven by a RS-422 transceiver in order to ensure that lines with length up to 10 m can be driven. The type of communication interface, UART or SPI, is jumper selectable during assembly of the unit. The baud rate of the APS+ UART is fixed at 115.2 kBaud.

IV. DISCUSSION

A limited performance test was done on the miniDSS, as well as a limited thermal vacuum (TVAC) test.

The misalignment of the aperture with respect to the APS+ chip in the x -direction was found to be $-11 \mu\text{m}$, while the misalignment in the y -direction was $4.5 \mu\text{m}$. These misalignment values fall within the expected manufacturing accuracy and would result in a worst case error of 0.28° if not compensated for by a limited calibration step. The misalignment values of the aperture in x - and y - direction were not notably affected by the TVAC test.

The field of view (FOV) was determined in a sun simulator at 1 solar constant (SC), by scanning across both perpendicular axes consecutively with a resolution of 2° until 50° and with a resolution of 1° from there on. The measured field of view is $102^\circ \times 102^\circ$. The field of view was found to be practically square, i.e. sun presence was for instance during a diagonal scan lost at $\alpha, \beta = 49^\circ$, a mere 2° less than when scanning on the α or β axis. By changing the FOV parameter by telecommand, a FOV can be selected from $102^\circ \times 102^\circ$, $91^\circ \times 91^\circ$, $69^\circ \times 69^\circ$ and $38^\circ \times 38^\circ$.

The resolution was determined by scanning on the α -axis with steps of 0.1° between -1° and 1° . The resolution was obtained by dividing the 0.1° angle step by the average change in Y -value as result of the 0.1° steps. The resolution was found to be 0.007° . The accuracy is not limited by the resolution, i.e. other factors are dominant in causing the errors that limit the accuracy. At present, a higher resolution, e.g. obtained from employing a larger number of pixels, would not improve accuracy.

The noise equivalent angle (NEA) was determined using an ensemble of measurements taken at 3 different locations in the FOV. The NEA was found to be 0.01° (3σ).

The APS+ chip must be positioned at a well-known and stable distance behind the aperture. The distance between the chip and the aperture (i.e. collimator height h) is a key parameter in the conversion from pixel coordinates to solar aspect angles. The larger its stability in time and with temperature, the better the sensor performance will be. In the miniDSS this distance is controlled by a ceramic spacer, adhered to the ceramic chip carrier on one side and to the sapphire mask carrier on the other side. In this way, a very stable sensor is obtained with materials that have a perfect match of their coefficients of thermal expansion (CTE). In order to test, among others, the temperature stability of the collimator height, a TVAC test was performed. The results of this test are shown in Figure 8. This graph shows errors in sun aspect angle α , i.e. the difference between the angle measured by the miniDSS and the angle at which light was applied to the miniDSS. The errors were measured during scans across the FOV in vacuum at three different temperatures: -15°C , 25°C and 50°C . As can be seen, the measured errors vary slightly with temperature and the temperature effect is largest at the edges of the FOV, as can be expected since the error is more sensitive to variations in h in those regions. However, the temperature effects are limited and never exceed roughly 0.02° when reducing or increasing temperature from room temperature. Moreover, across the FOV and at all temperatures, the error never exceeds 0.03° , indicating that the accuracy, at least on the α -axis, is about 0.03° . Further measurements are required to confirm that this accuracy is achieved across the complete FOV. It should be noted that the errors are rather systematic in nature, suggesting that an even higher accuracy could be achieved, albeit at increased calibration costs, if a full calibration LUT were to be used by the S/C. This high accuracy combined with albedo insensitivity and low production cost, mass and power consumption suggest that the miniDSS could, in combination with other sensor units, also be used in AOCS modes other than safe mode or sun

acquisition mode, such as modes where a moderately high pointing accuracy is required.

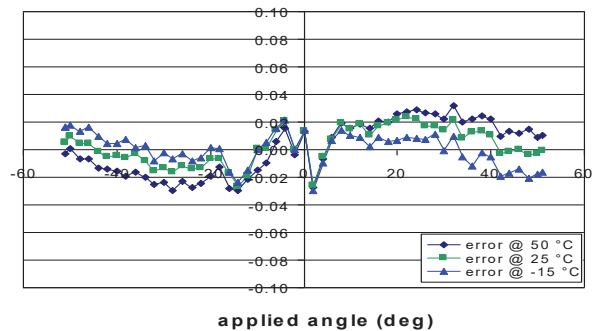


Figure 8: Errors in sun aspect angle α measured during scans across the FOV in vacuum at different temperatures.

The miniDSS design was specifically optimized for low power consumption. The power consumption was measured to be only 65 mW, which is roughly a factor 15 lower than found in conventional high-precision digital sun sensors [1, 2]. Moreover, the power consumption was found to be practically independent of the operating mode. At dimensions of $69 \times 52 \times 14 \text{ mm}^3$ and a mass of only 72 grams, the miniDSS has achieved an extreme reduction in both volume and weight as compared to the conventional devices, i.e. roughly a factor 10 and 5, respectively.

V. CONCLUSION

A high-precision low-power miniaturized digital sun sensor has been developed at TNO. The miniDSS is a single chip sun sensor comprising an ASIC with a APS detector. The sensor is effectively albedo insensitive and the design was optimized for low recurrent cost. The prototype combines an accuracy in the order of 0.03° with a mass of just 72 g and a power consumption of only 65 mW. This high accuracy combined with albedo insensitivity and low production cost, mass and power consumption suggest that the miniDSS could also be used in AOCS modes where a moderately high pointing accuracy is required. The miniDSS prototype is expected to be launched on QuadSat in 2012 for in-orbit demonstration.

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