Heterogeneous Integration of Semiconductor Materials: Basic Issues, Current Progress, and Future Challenges.

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ABSTRACT

The world's dominant IC material, silicon, cannot do everything we want a semiconductor material to do. However, for this discussion, the fact that Si wafers are of high quality, large and cheap is of great interest. This is important for at least two reasons. First, nearly all of the electronic and photonic compound semiconductor devices that comprise the current $20 billion per year market are fabricated on substrates that are either very expensive or non-optimal for the epitaxy required to realize the device or an IC of interest. A second reason is the integration of new functionality to current Si technology. Clearly, if many of the current photonic applications already realized in current compound semiconductor technology could be integrated into Si technology, some of the herculean efforts to continue following Moore's Law (including trying to do it via nanotechnology) could be mitigated. This presentation examines some of the basic materials science issues involved with heterogeneous integration of semiconductor materials. These include those applications in which the active device region requires a high degree of crystal perfection and those that do not. Epitaxy issues at the hetero-interface, heterovalent versus homovalent epigrowth, and dislocation dynamics are presented. Notable historical examples are summarized, followed by examples of current successful approaches including the materials science concepts used to achieve the results. A list is made of some challenges that need to be solved in order to continue making future progress.

Keywords: heterogeneous integration, defects. interfaces. GaP on Si.

1. INTRODUCTION

A discussion about heterogeneous integration (HI) of semiconductor materials and devices is warranted because the world's most important electronic material, silicon, has functionality limitations. For example, it cannot be used for bright and efficient LEDs of all colors, lasers of all colors, high efficiency power devices, and applications in extreme environments, just to name a few. However, thanks to Moore's law, it has provided electronic ICs, at a density of greater than a billion transistors per chip and a worldwide market of over $300 billion[1]. However, missing is electronic and photonic integration; and the successful integration of compound semiconductor superstrates for discrete device applications.

More importantly, in order to achieve an optimal price-performance ratio for IC chips, semiconductor engineers learned how to make high quality Si wafers with a wafer diameter of 12 inches and at a cost of less than $50 per wafer[2]. This is important for at least two reasons. First, nearly all of the electronic and photonic compound semiconductor devices that comprise the current $20 billion per year market are fabricated on substrates that are either very expensive or non-optimal for the epitaxy required to realize the device or an IC of interest. HI of these devices on cheap Si substrates could be of interest.

For example, the latest one sun efficiency record using a single material solar cell is not held by Si, but by a GaAs based heterojunction structure. Even though the epilayer cost is sufficiently low to realize a cost goal of $1/W[3], if the GaAs substrate material is included in the cell, there is no way this goal can be achieved. Also consider the case for III-N LED photonics and microwave power technology; there are no commercially available substrates to realize the state-of-the-art laboratory results in the manufacturing arena, especially if multifunctional ICs are desired. Therefore, the economics of scale using Si substrates for epilayer depositions might enable future applications now precluded owing to adverse price-performance ratios using current substrate technology.

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A second reason for using Si technology is the integration of new functionality to current Si technology. Clearly, if many of the current photonic applications already realized in current compound semiconductor technology could be integrated into Si technology, some of the herculean efforts to continue following Moore's Law (including trying to do it via nanotechnology) could be mitigated.

The purpose of this manuscript is to present an overview of some of the basic materials science issues associated with HI of semiconductor materials. The currently important forms of heterogeneous integration including liftoff, shear removal, and heteoepitaxy will be discussed in terms of those applications in which the active device region requires a high degree of crystal perfection and those that do not. Epitaxy issues at the hetero-interface, heterovalent versus homovalent epigrowth, and dislocation dynamics will be presented. Finally, some of the challenges that need to be solved in order to achieve future progress will be listed. The reader is advised that examples and figures not presented in the manuscript will be given in the oral presentation at the conference.

2. HETEROGENEOUS INTEGRATION

2.1 HI Defined

For the purpose of this discussion, HI is defined as the joining together of two or more chemically distinct semiconductor materials for the purpose of realizing new chip functionality or improved photonic and electronic devices. The following will serve as defining examples: AlGaAs/GaAs, Si/SiO_2, SiO_2/Si, HfO/Si, Si/Al_20_3, SiC/Al_2O_3, Si/GaP, GaN/Al_2O_3, GaN/Si, ZnO/InP, etc. In fact the list is almost innumerable, since nearly over 95% of current semiconductor devices, chips and circuits in the market place are heterogeneously integrated. The fundamental question here is what are the current limitations for realizing device quality HI of anything on anything else.

2.2 A Multi-dimensional Issue

To answer the last question we need to understand that HI is a multi-dimensional issue. The coordinates are: 1) methods of HI; 2) interface crystal structure and electronic properties; 3) interface chemistry, abruptness, and functionality; and 4) circuit versus discrete applications. These coordinates will be discussed and a couple of current emerging successes will be presented. No attempt is made to either include or to address the subtle details of all possible examples found in the literature.

3. DIMENSIONS OF HETEROGENEOUS INTEGRATION

3.1 Methods of HI

The methods discussed here are epitaxy, thin film deposition, and thin film transfer. The following discussion is meant to be exemplary rather than exhaustive.

Epitaxy in the context of HI means heteroepitaxy and is the currently most utilized method used to achieve HI. The menu of major methods of epitaxy includes[4]: 1) chemical vapor deposition (CVD) and vapor phase epitaxy (VPE), in which a vapor phase chemical reaction occurs at a substrate surface; 2) physical vapor deposition (PVD) with its many variants; 3) liquid phase epitaxy (LPE); and solid phase epitaxy (SPE). Examples of CVD and VPE include silane (SiH_4) and silicon tetrachloride ($SiCl_4$) vapor phase decomposition to produce Si epitaxial layers. Examples of compound semiconductor, e.g. GaAs, vapor phase chemistry are arsenic trichloride ($AsCl_3$) plus Ga or trimethyl gallium ($Ga(CH_3)$) plus arsenide (AsH_3) reactions to form epilayers of GaAs. The latter process is also known as metal-organic-CVD (MOCVPE). This method has the advantage that most of the group three elements will easily form with the trimethly or triethyl radical, thus can serve as a "universal" source for III-V epitaxial systems.

In the field of PVD[4], perhaps molecular beam epitaxy (MBE) stands out as the current salient technology. MBE is simply forming epitaxial layers via thermal evaporation (PVD), usually elemental source, e.g. Ga and As for GaAs. MBE is differentiated from PVD in two ways. First the substrate is heated to allow the physisorbed ad-atoms, e.g. Ga and As, to find an appropriate epitaxial site and chemically bond with an atomic crystal registration the same as or commensurate with the substrate. This epitaxial bonding registration is a key component in achieving HI when low defect densities are required at both the HI interface and in the epilayer. The second distinction of MBE is its ultra-high vacuum environment. This is required, since parts per million incorporation of extraneous material in the epilayer, e.g. oxygen, water, etc., can result in a useless device. While MBE is widely used in the production of compound semiconductor devices, its most valuable feature is that research materials can be fabricated without having to depend on the availability of precursor vapor phase chemicals.

There are now emerging new classes of PVD methods that are being developed to assist in broadening the menu of new systems available for HI applications. A partial list includes: atomic layer deposition (ALD)[5] and several variants, pulsed laser deposition (PLD)[6], and plasma enhanced ALD (PEALD)[7]. They all have a common feature: to overcome limitations associated with applying the established methods to new materials for device applications. It should be noted that these techniques are in some cases subtle modifications of a multitude of commercial techniques which are successful in fabricating thin films which are either polycrystalline or amorphous in structure.

It should be noted for historical accuracy that the subclass of HI derived devices known as lattice-matched heterojunctions (HJs), was not originally enabled by any of the above techniques. Rather, they were invented, perfected and manufactured by the LPE method[4,8]. (The devices realized by LPE and pioneered by the author of this paper include the ultra bright red LED, the heterojunction bipolar transistor (HBT), the high efficiency heterojunction solar cell, and the pseudomorphic high electron mobility transistor (P-HEMT) and others.) These were all realized using LPE to fabricate these devices structures using HJs of AlGaAs and GaAs.

Lastly, even though there currently is no widespread use of the SPE technique[4], it warrants a description here for possible future reference to those working in the field of HI. It works when an amorphous film is deposited on a suitable substrate. A film in the amorphous state has a higher free energy than when it is in the crystalline state. Thus, by applying thermal energy the amorphous film can be transformed to its lower crystalline state. An example of this is the recrystallization of a layer doped amorphous Si to incorporate low solubility dopants.

Thin film deposition is distinct from epitaxy in the sense that the resulting layer need not be crystalline nor have any epitaxial relationship with the underlying crystalline substrate or superstrate. Even though this topic is of a critical importance to the fabrication of devices, chips and ICs, especially for current contacts and device passivation and isolation, it will not be addressed in this discussion.

In addition to identifying an optimal HI solution via an epitaxy method, there is considerable current activity whose goal is to epitaxially deposit highly perfect device structures on an optimal substrate, e.g. AlGaAs or GaInP on a GaAs substrate, and then transfer the device from the optimal substrate and bond it to another wafer carrier, e.g. glass or plastic, or onto, for example, a Si IC. There are two basic approaches used to achieve this: chemically assisted lift-off separation, and mechanical shear separation.

Lift off is accomplished by depositing a sacrificial layer onto an optimal substrate that can be selectively removed by chemically selective etching. An example of this approach was pioneered by the author[9], and subsequently developed by Yablonovitch, et. al.[10], is to deposit a lattice-matched, highly perfect layer of Al rich AlGaAs onto a GaAs substrate. This layer then serves as both the superstrate for the epitaxy of highly perfect lattice-matched device structures and as the sacrificial layer that will be subsequently removed by "lift off" via etching away the sacrificial layer using either HCl or HF acids. This so called lift off technique is of great current interest in the photovoltaics community as a pathway to achieve the target cost goals for deployment of cost competitive, global scale solar cell systems. This is because the current

systems target capital cost of $1/W cannot be met if the solar cell must include the substrate on which it is deposited. This is also true for Si PVs. The lift-off technique, supposedly holds the promise of cost effective high efficiency GaAs based cells that can be used in systems that require only modest non tracking solar concentration. The key to its success will be the actual ability to reuse a given substrate enough times to amortize its cost by the required amount. It is ironic that the current record for single-junction solar cell efficiency is held by GaAs based cells made by the lift off method.

The down side to this approach is the integration of high speed, high power, or photonic compound semiconductor devices as peripherals onto Si ICs. The combination of lift off and micron scale registration of these peripheral devices can be daunting.

This problem may be mitigated by the mechanical shearing separation technique being pioneered by Islam, et. al.[11]. He and his group have invented a clever way of realizing highly ordered 3-D arrays of electrically isolated nano-scale pillars of high quality Si. The key to this technique is to form a 3-D array of nano wires on a Si substrate and then transfer them by mechanically shearing them, vertically intact, to another carrier, usually an insulating polymer. This technique has the significant advantage of being able to fabricate vertical 3-D arrays of high quality material, thus, offering a pathway to achieve the holy grail of fabricating ICs of electrically isolated spatially ordered arrays of nano wire devices and circuits.

3.2 Interfaces: Structure, Perfection, Chemistry, and Electronic Properties

For nearly all HI applications the interface crystal structure is probably the most critically important issue. It will determine both the crystal perfection between layers of a device structure and between the substrate or superstrate and the epilayer. This in turn will determine the electronic properties associated with charge transport. If there is strain involved the chemistry of interfaces will also be affected.

Lattice-matched isovalent HJ interfaces are the simplest example of the multi-dimensional complexity issues of the HI of HJs. Well-studied examples of this type of interface include AlGaAs/GaAs, lattice matched GaInP/GaAs, and InP/InGaAs interfaces. Using the established epilayer growth methods described above, it is possible to make nearly ideal interfaces. This interface is nearly lattice matched and nearly strain free. Therefore, since there is no change in valency across this interface, hence, no extraneous charges in the interface, the charge carrier transport and photonic properties are nearly ideal, and can be accurately modeled using the concepts of known semiconductor physics. Of particular interest are the conduction and valence band offsets, which determine both photonic and charge carrier transport properties of the structure. Once material scientists learned how to make ideal heterojunctions, commercially important devices such as, LEDs lasers, HBTs solar cells, HEMTs and others quickly appeared in the marketplace. In fact the current worldwide market for compound semiconductor HJ devices is about $20 billion per year and growing. However, it needs to be emphasized that even though these interfaces can be ideal, their ideality is strongly dependent on the epitaxial environment. In particular, even a low background concentration of oxygen bearing contaminates during epitaxy will degrade ideal electronic and photonic properties both at an interface and the epilayer itself.

The next level of complexity for interfaces is the non-lattice-matched isovalent interface. There are two structural configurations for these interfaces. One is if the strain due to mismatch is small and is not relieved, known as a pseudomorphic interface. The electronic and photonic properties of this type of interface can be modeled as ideal by accounting only for the effect of strain on the interface. For low strain conditions, as, for example, the Ga rich InGaAs/GaAs pseudomorphic interfaces, the electrical and photonic properties nearly match those for ideal isovalent lattice-matched HJs. As a result, pseudomorphic HJ devices are currently on the menu of commercially available devices. However, if the strain is relieved between the substrate and epilayer or between mismatched epilayers the resulting structural, electronic and photonic properties are vastly different than interfaces between lattice-matched layers. This condition is described as a metamorphic interface. If the strain is small, the dynamics of epitaxy begin with the formation of a pseudomorphic layer. If growth continues to the point of the epilayer being thicker than a threshold thickness, known as the critical thickness, the strained layer will relax back to its equilibrium

lattice constant. The relaxation is usually mediated by the formation of glide dislocations that migrate to the mismatched interface. Depending on the epitaxy technique employed, the relaxed layer will either contain threading dislocations or be dislocation free. As a result of the planar array morphology of the interface dislocations, the electronic properties at the interface will be vastly different from the band offset modeled results observed for pseudomorphic interfaces in many III-V systems. In contrast, there are electronic states associated with the glide and threading dislocations that pin the Fermi level at some characteristic energy, and dominate the band offset physics at the heterojunction interface[12].

This can either be beneficial or detrimental on device function and performance. For example, at the metamorphic Ga rich GaInAs/GaAs interface, the states in the dislocation pin the Fermi level at an energy near mid gap and cause band bending near the interface of doped structures. This band bending will drift minority carriers into the dislocation states and render minority carrier devices such as, LEDs, lasers, HBTs, and solar cells either inoperable or having insufficient performance. On the other hand, for majority carrier devices such as Schottky diodes, and MESFETs, the presence of interface dislocations and the resulting interface Fermi level pinning, could actually improve device performance. An example of the beneficial aspects of having the interface electronic properties determined by a high density of interface sessile dislocations are the thermally stable Schottky barriers (compared with metals) that occur when InAs is deposited on GaAs[13]. Sessile type dislocations are discussed below.

The growth and properties of large lattice-mismatched isovalent interface systems are very different from those of small lattice-mismatched interface, especially in the dynamics of epitaxy and dislocation structure. For large lattice mismatch interfaces, the strain is sufficiently large that 2-D pseudomorphic growth does not occur. Owing to the thermodynamics associated with achieving a minimum in free energy at strained interfaces, metamorphic 3-D nucleation takes precedence over pseudomorphic 2-D nucleation. Instead, the deposited 3-D nuclei are already nearly relaxed by the mass flow formation of sessile dislocations under the nuclei at the interface. As the epilayer growth continues, the 3-D nuclei enlarge and merge together and the epitaxy mode changes from 3-D to 2-D. Since the sessile dislocations at the interface that formed during initial nucleation are not necessary in registration between the nuclei, when nuclei merging does occur, any misaligned interface dislocation will bend up into the epilayer as the epilayer mode becomes 2-D. Dislocations that propagate into the growing epilayer are usually of the threading type. However, since dislocation type can depend on the materials system and growth technique, this topic will not be discussed further here. The InAs/GaP mismatched interface is a notable example of the electronic properties that can occur at isovalent interfaces with a large difference in lattice constant. It was found that states associated with in-plane interface crossings of sessile dislocations had energies close to the conduction band of InAs, and thus contributed to n-type doping in the InAs layer via defect states rather than by doping.

The definition of small versus large mismatch is somewhat arbitrary and can depend on the epitaxy method employed. An example of this is the MBE of InGaAs on GaAs. For Ga rich InGaAs layers, epitaxy proceeds pseudomorphically as it would for the small lattice-mismatch regimes. For In rich InGaAs layers grown on GaAs growth proceeds by the 3-D nucleation mode expected for large lattice mismatched systems.

The topic of managing dislocations resulting from non-lattice matched epitaxy is a topic of current intense R&D activity. The reason for this is due to the fact that except for pure Si based devices, which can be fabricated on high quality, large diameter Si wafer substrates, there are many other desired device performance parameters that are dependent on materials with optimal optical properties and optimal transport properties for which there are no readily available lattice matched substrates. This means technologists must cope with the current substrate menu and figure out how to accomplish successful dislocation management.

In addition to detrimental dislocation effects at non-lattice matched interfaces, there is another equally important issue that needs further study; the effect of internal strain on alloys. For alloys formed in nearly lattice and thermal expansion matched binary compound semiconductor materials, e.g. AlGaAs, it is possible to form completely miscible and stable compositions between GaAs and AlAs. In contrast, it has

been observed that for alloys formed in non lattice or thermal expansion matched compound semiconductor materials, e.g. GaInP and GaInN, the resulting internal strain can cause phase separation, e.g. GaInN decomposing into phases of Ga rich GaInN plus In rich GaInN, thus precluding the ability to realize homogeneous epilayers with the desired optical and electrical properties. The limitations of stable compositions in the GaInP and GaInN systems have been reported. The good news is that epilayer growth conditions may have been found that allow a full range of single-phase compositions between GaN and InN[14]. The not so good news is that the high band gap composition regions of GaInP may not be readily accessible[15].

Perhaps the most important level of complexity is the lattice-matched heterovalent interface, whose poster child is the GaP/Si heterojunction. The reason for this is that the GaP/Si interface represents a pathway to achieve the holy grail of the heterogeneous integration of peripheral compound semiconductor photonic, high speed and high power devices with Si CMOS technology. Even though there is lattice matching at the interface the complexity is maintaining charge neutrality across the heterovalent interface, i.e. covalent bonding with no interface charges. Remember that semiconductors are covalently bonded and that a surface atom of the host semiconductor has to find an ad-atom that maintains charge neutrality upon bonding with the host's surface atom. Obviously, when a Si atom becomes an ad-atom on a Si surface and bonds with the host atoms, the octal valency required for diamond crystal structure neutrality is satisfied. Likewise, if a GaAs surface is terminated with Ga atoms during epitaxy, an As ad-atom will easily bond with the Ga surface atoms; again satisfying the octal valency required for zincblende crystal structure neutrality.

However, when a P or Ga ad-atom tries to bond with a Si surface atom a planar charge dipole layer will form that will produce an electric field of sufficient magnitude to break covalent bonds and to prevent Ga-Si or P-Si bonded planar layers from forming. As a result, there have been no reproducible reports of 2-D nucleation layers of GaP on Si. Rather, only 3-D nucleation layers have been consistently reported in the literature. Also there is an additional complexity associated with heterovalent epitaxy. Imagine an atomically flat Si surface where there is an occasional monolayer step in the surface. Now imagine both P ad-atoms and Ga ad-atoms impinging the surface. Suppose Ga ad-atoms bond in one area of the surface and P ad-atoms bond in another area separated from the first area by a monolayer step in the Si surface. As the GaP layer begins to thicken and propagate laterally, the two propagating GaP layers will meet at a monolayer step and the GaP layers on each side of the step will be out of registration, e.g. Ga atoms will be juxtaposed with Ga atoms on the other side of the step, and thus be in an anti-bonding state. The intersection formed by this misalignment is called an anti-phase boundary (APB) and has been widely studied in the literature. It has been also reported that the electronic properties of the bulk material can be altered by APBs. Clearly, from a crystal perfection point of view APBs are undesirable. Therefore, there has been significant work in the literature to eliminate their formation during epitaxy. There is a consensus that the elimination of APDs is best achieved by preparing wafer substrates for heterovalent epitaxy with the wafer misaligned by a few degrees from major crystallographic orientations, e.g. (100), (110), (111) planes.

Within the last couple of years, workers[16,17] have reported success in achieving 2-D nucleation of GaP on Si. The details are best revealed by reference to the cited publications, and the author recommends that interested readers review the work by Volz, et. al.[16], in particular. However, among the key steps of successful epitaxial procedures, one involves depositing a buffer layer of epitaxial Si on the Si substrate before the in situ continuation of the epitaxy step used for the nucleation of the 2-D GaP layers. If other workers succeed in reproducing these results, it will represent an important step in realizing heterogeneous integration of semiconductor materials. Specifically, being able to have a defect free layer of GaP on Si means low cost, large area GaP superstrates will replace the need for bulk GaP crystals in the future.

Perhaps, the greatest challenge facing the epitaxial deposition industry is the heterovalent non-lattice matched interface. This needs to be addressed because a major developing industry already uses this type of interface to fabricate blue and green lasers, as well as blue, green, UV and white LEDs. A most unlikely materials combination of III-Nitrides, and sapphire substrates have enabled this industry[18]. Specifically, GaN, GaInN, AlGaN and AlInN are epitaxially deposited on single crystal alumina substrates. The

development of this industry has the same history as the Si chip industry; the technology preceded the underlying materials and devices science; products happened by empirical experimentation, i.e. technologists just tried it and it worked. Since the materials science in this field is ongoing and somewhat disjointed, it is beyond the scope of this article to describe it in detail. However, it can be generally said that in addition to the previously complexities discussed previously, bonding chemistry across the interface and defect management becomes of critical importance.

3.3 Interface Chemistry, Abruptness and Functionality

In addition to issues of crystal structure and electronic properties of interfaces, there needs to be a short discussion about interface chemistry and interface abruptness. When considering HI methodologies, either by lift-off, epitaxy, or shear separation, interface chemistry or abruptness must be considered. If there is a chance of reaction chemistry it needs to be determined if it is helpful or detrimental.

It is important to note the electronic differences between abrupt and compositionally graded interfaces. When two semiconductors are abruptly joined together and have differing band gaps and electron affinities there will be a discontinuity in the band edges, i.e. either a conduction band offset or a valence band offset or both, at the interface. If the interface is electronically perfect i.e. no interface states, and the work function of both materials is the same, there will be an abrupt change in the electrostatic potential at each band offset. If the workfunctions are different due, for example, to doping, there will be charge transfer across the interface. The famous high electron mobility transistor (HEMT) has a very high charge carrier velocity in the channel as a result of electron flow from the doped AlGaAs layer into the GaAs channel.

If there are defects at the interface that cause interface Fermi level pinning, in addition to the electrostatics of band offsets, there will usually be an undesirable charge carrier transport into the defect states. This situation usually occurs at lattice-mismatched interfaces, surfaces, and grain boundaries and usually results in minority carrier devices with insufficient performance.

One of the early successes of LPE was its inherent ability to form graded HJs[19]. Grading HJs will also grade out the abrupt change in electrostatic potential that occurs at abrupt HJs. Even though the abrupt HJ is a critical feature of HEMTs, abrupt band offsets can limit performance in HBTs and other HJ based devices. Therefore from a functionality perspective, abrupt HJs are needed for majority carrier transfer devices, tunneling devices, quantum well lasers and quantum dot devices. However, graded HJ are preferred for many minority carrier devices, like HBTs, where the abrupt band offsets can degrade performance.

There are two currently important commercial examples of the importance of the role of interface chemistry: Si based MOSFETs and III-N based photonic and electronic devices. The current commercial Si MOSFET technology would not exist had it not been for the discovery of the chemistry cure for the unsuitable electronic properties at the native SiO_2/Si interface, i.e. the dangling chemical bonds which cause interface electronic states. Miraculously, the simple act of protonating the interface eliminated the interface states and enabled the current $300 billion/year industry! The HfO/Si interface is still being investigated to determine why this interface is nearly electronically ideal.

There is a different chemical miracle that has enabled the current III-N LED, laser, and electronics industry. When the surface of a low index plane of single crystal substrate of Al_2O_3 (alumina) is structurally examined the surface is found to be passivated, i.e. there is not a significant density of dangling bonds present. Since alumina molecules and crystals have strong chemical bands and the surface is passivated it appeared to be a thermodynamic miracle that highly defected, yet operable, III-N devices could be realized by epitaxy of III-Ns on alumina substrates. It was found that the key to nucleation of III-N epitaxial structures is the reaction of the nitrogen atom with the Al_2O_3 surface. A preferred initial nucleation step for III-N epitaxy technology is the exposure of plasma-activated nitrogen to a heated alumina substrate. The thermodynamic miracle is that the AlN bond is stronger than the AlO bond. Hence, III-N nucleation is accomplished via a replacement reaction of O with N at the alumina surface. More recently III-N HI has

been achieved via both Si and SiC. However, understanding the materials science of these technologies is beyond the scope of this presentation. On the other hand there are a couple of historically interesting examples of non-lattice matched heterovalent epitaxial investigations that will be presented here.

One of the important operational issues in any IC is the ability to achieve electrical isolation between active devices. This is a particularly onerous problem with Si ICs because intrinsic Si, even though resistive, is not a suitable insulating material. Therefore, in the 1970s researchers investigated depositing epitaxial Si FETs on single crystal substrates of alumina. Even though the transistors worked they exhibited inferior performance compared to devices fabricated on Si substrates. It is noted that even though the isolation issues were mitigated through circuit design, there is current work in this field aimed at improving performance in future high density IC chips. It is also noted in passing that during the late 1950s IBM had a significant research program aimed at fabricating Ge based transistors on semi-insulating GaAs substrates. There was some technical success, but Si won the race owing to the superior electronic properties of silicon dioxide on Si compared with the inferior passivation properties of germanium oxide on Ge.

3.4 Discrete Versus Integrated Function and Future Challenges

The discussion about discrete integration usually involves two issues: the availability of lattice matched substrates and their cost relative to the worth of the discrete device application under investigation. Generally, for discrete device applications for which there exists lattice matched substrate, e.g. AlGaAs, and GaInP grown on GaAs substrates for discrete LEDs, lasers, HBTs, HEMTs, etc., the per device area of the GaAs substrate is insignificant compared with the value of the packaged devices. On the other hand the situation is completely different for GaAs based flat plate solar arrays whose device cost needs to be under $1/watt. Even if the cost of the active epilayer part of the solar cell can achieve this cost target, the system cost target cannot be accomplished if the GaAs substrate is included in the array. This fact has led companies like the Alta Devices, a solar cell company, to adopt a business plan that fabricates state-of-the-art efficient GaAlAs/GaAs epilayer cells on GaAs substrate and then by the lift-off technique, transfer the cells to a thin flexible, transparent and low cost material. The hope is that the GaAs substrate can be reused a sufficient number of times to amortize its initial cost away. In contrast the business plan of First Solar is to commercialize a polycrystalline based CdTe cell deposited by a low cost, large area coating process and still yield the necessary solar power to electric power conversions needed for economic competitiveness. At this time the jury is out on the probable success of either of these approaches.

Another aspect of discrete device technologies concerns the lack of reliable and sustainably available highly perfect, low cost lattice-matched substrates. For example, only laboratory scale GaN substrates are currently available. It is not clear at this time if a viable GaN substrate technology will emerge from the laboratory. This lack of certainty could be a major driver for the development of discrete device technology that employs HI with Si substrates. This had already happened for the devices built on GaP. Even though these substrates are commercially available several laboratories are developing HI of GaP superstrates on Si.

As previously discussed, there is a great incentive to be able to realize HI using high performance peripherals such as lasers, LEDs and high power devices made of non-silicon materials, and extend current Si CMOS technology to include more complexity and functionality. There have been recent advances that might realize this goal. The reader is again referred to Volz et. al. to gain a comprehensive knowledge of the status of this progress.

Finally, the author includes a personal list of important challenges that need addressing to see the promise of HI fulfilled.

1. Production scale demonstrations of the HI of 2-D highly perfect GaP superstates on Si.
2. Realization of the menu of currently important compound semiconductor devices on GaP superstates made on a production scale.
3. A large scale, economically and commercially viable GaN substrate technology.
4. Production scale demonstration of an economically viable epilayer separation and re-bond technology.

5. Consensus in the technology community about the viability of managing phase separation issues in highly strained systems, e.g. GaInN.

4. CONCLUDING REMARKS

There has been significant and very recent progress towards realizing commercially viable HI technologies. Some of this progress and the underlying materials science issues have been presented here. However, as has happened in the past, potential breakthroughs could languish in the journals unless the technology community can move these breakthroughs into the production arena. Otherwise, the less than optimal incumbent technologies will continue to rule.

REFERENCES

[1] http://www.euroasiasemiconductor.com/article/74874-Slow-Growth-Expected-for-Worldwide-Chip-Market-2012.php
[2] http://compare.ebay.com/like/360363024909?_lwgsi=y&ltyp=AllFixedPriceItemTypes&var=sbar
[3] http://www.isuppli.com/Photovoltaics/News/Pages/Historic-1-Per-Watt-Solar-Modules-Just-Months-Away.aspx
[4] http://en.wikipedia.org/wiki/Epitaxy
[5] http://en.wikipedia.org/wiki/Atomic_layer_deposition
[6] http://en.wikipedia.org/wiki/Pulsed_laser_deposition
[7] http://avspublications.org/jvstb/resource/1/jvtbd9/v18/i4/p2016_s1?isAuthorized=no
[8] Woodall, J. M., Rupprecht, H., and Reuter, W., "Liquid Phase Epitaxial Growth of $Ga_{1-x}Al_x$ As," J. Electrochem. Soc., 116, 899-903 (1969).
[9] Stern, F., and Woodall, J. M., "Photon Recycling in Semiconductor Lasers," J. Appl. Phys., 45, 3904-3906 (1974).
[10] Yablonovitch, E., "Ultra-Efficient Liftoff Solar Cells Exploiting Optical Confinement in the Wave Limit," NREL/SR -520-26903, Final Report, 1-6 (1999).
[11] Logeeswaran, V. J., Katzenmeyer, A. M., and Islam, M. S., "Harvesting and Transferring Vertical Device Arrays of Single Crystal Semiconductor Micro/Nanopillars to Arbitrary Substrates," IEEE Trans on Electron. Devices, 5(8}, 1856-1866, 2010.
[12] Woodall, J. M., Pettit, G. D., Jackson, T. N., Lanza, C.. Kavanagh, K. L., and Mayer,J. W., "Fermi-Level Pinning by Misfit Dislocations at GaAs Interfaces," Phys. Rev. Lett., 51 1783-1785 (1983).
[13] Gopal, V., Kvam, E. P., Chin, T. P., and Woodall, J. M., "Evidence for Misfit Dislocation-Related Carrier Accumulation at the InAs/GaP Heterointerface," Appl. Phys. Lett. 72 2319-2321 (1998).
[14] Moseley, M., Lowder, J., Billingsley, D., Doolittle, W. A., "Control of Surface Ad-atom Kinetics for the Growth of High-Indium Content InGaN Throughout the Miscibility Gap.", Appl. Phys. Lett., 10 191902(1-3) (2010).
[15] Fitzgerald, E. A., private communication, 2010.
[16] Volz, K.,Beyer, A., Wiebke, W., Ohlmann, J., Nemeth, I., Kunert, B., and Stolz, W., "GaP-Nucleation on Exact Si (001) Substrates for III/V Device Integration," J .Cryst. Growth, 315 37-47 (2011).
[17] Grassman, T. J., Brenner, M. R., Rajagopalan, S., Unocic, R., Dehoff, R., Mills, H., Fraser, H., Ringel, S. A., "Control and Elimination of Nucleation-Related Defects in GaP/Si (001) Heteroepitaxy, Appl. Phys. Lett., 94 232106-1-3 (2009).
[18] http://en.wikipedia.org/wiki/Gallium_nitride
[19] Woodall, J. M., Potemski, R. M., Blum, S. E., and Lynch, R., "Ga1-xAlxAs LED Structures Grown on GaP Substrates." Appl. Phys. Lett., 20 375-377 (1972).