In-design and signoff lithography physical analysis for 7/5nm

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ABSTRACT

At advanced nodes, definition of design rules and process options must be tightly optimized to deliver the best tradeoff performance, power, area and manufacturability. However, implementation platforms don't typically have access to process information and process teams don't have complete design knowledge. Also, optimization loops required for Design-Technology-Co-Optimization (DTCO) are either impossible or at best long and expensive for fabless design house.

Joining forces, ASML, IMEC and Cadence Design Systems developed an In-design and signoff lithography physical analysis well suited for 7/5nm and below. The Tachyon OPC+ and LMC engines used by IMEC 7/5nm process has been integrated in Cadence Litho Physical Analyzer (LPA) to perform lithography checks using the foundry process models, recipes, and hotspot detectors. This flow leverages existing LPA infrastructure for both custom and digital design platforms, as well as standalone signoff.

Depending upon the end application, LPA could be launched either from place & route, custom layout or standalone. LPA PLUS processes first the design database to identify hierarchy, decompose the layout for coloring and apply pattern matching to identify location requiring simulation. The layout is then passed to the Tachyon OPC+ engine to perform optical proximity correction and to Tachyon LMC engine for model-based litho verification that is validated on Silicon. The hotspots and contours are processed by LPA PLUS for generation of hotspot marker and fixing guidelines. It then provides all this information to the design environment.

The flow has been developed and demonstrated to work on IMEC 7nm, and can be ported to smaller or larger technologies. This paper will present the result of this In-design and signoff lithography physical analysis flow, how DTCO and design teams can add manufacturability to PPA.

Keywords: OPC, lithography, 7nm, 5nm, DTCO, DFM

1. INTRODUCTION

Proximity effects have an ever growing impact in physical design as the continued scaling has driven the lithography k1 down. This has resulted in dramatic increase in design rule counts and the strong interaction of proximity effects and hotspots appearing in the design[1]. Stochastic variation and overlay sensitive hotspots are also critical to account for during the development of the physical design rules and these variation sources together with proximity dominate the total EPE variation budget[2] as shown in Figure 1.

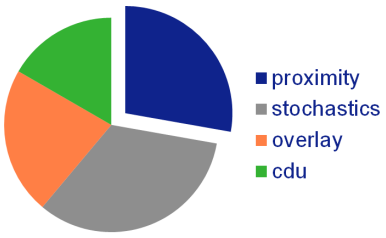

Figure 1. Proximity is a large part of the total edge placement error budget and together with stochastic and overlay make up over 75% of the budget.

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Part of the reason for the growing importance of proximity effects has come from the continued scaling without resolution improvements in lithography. Looking at the past decade of immersion lithography shows standard cell sizes scaling from ~2um to ~0.2um while the optical ambit has changed little. This is illustrated as with the visualization of the optical ambit and standard cells on 3 layouts at 45, 14, and 7nm nodes in Figure 2.

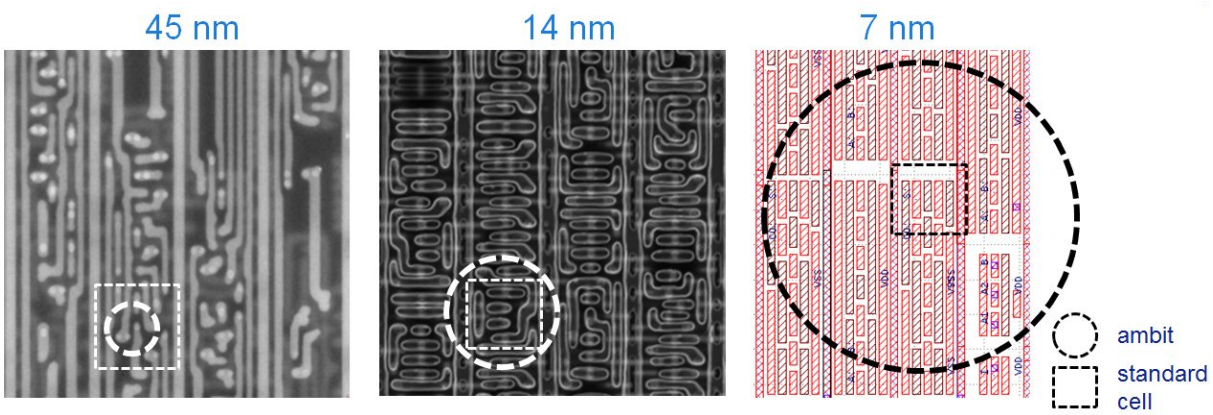

Figure 2. Optical diameter and standard cell size illustrated on 3 recent technology node layout images.

Sign off mask generation and verification flows enabled in the leading design environment for digital and custom designs is a valuable tool to quickly develop and improve manufacturability of designs at advanced process nodes. In addition, the development of the standard cell architecture, metallization stack and track plans, router setup and strategy, and many other parts of the design-technology co-optimization (DTCO) require access to lithography simulation in the design context. The state of the art Tachyon lithography simulation and correction ecosystem from ASML is now accessible in the design environment via LPA PLUS and enables manufacturability analysis directly from the design creation tools.

2. IN DESIGN HOTSPOT SEARCH AND REPAIR

Accurate and easy-to-use design manufacturability checks are key factors of successful design development. Designers demand solutions that can be easily integrated in the design environment and can deliver a desktop solution in a reasonable time. The solution from Cadence and ASML meets these requirements:

- Accuracy: By bringing the foundry certified models in the design environment, designers can access to accurate results without having to send their design to the foundry, and have results right back in their design environment.
- Ease of use: From the designer stand point, LPA use model does not change with the ASML integration. Cadence LPA was already readily available in Cadence Innovus digital implementation through a single command that launches the litho checks through scripting and bring back the hotspots found in the violation browser for designer review and more importantly for automated fixing. LPA in Innovus provides several fixing strategy, such as the basic rip-up –and-reroute to advanced surgical fixing guidelines. In Cadence Virtuoso custom design environment, LPA is also integrated through in the graphical layout design environment and designers can review the results in the annotation browser and perform fixing. LPA signoff is set with a simple configuration file pointing to the litho techfile coming from the foundry. Another aspect of ease-of-use is runtime. If OPC team can use thousands of CPUs and wait weeks for mask data to be ready, designers often cannot have this luxury. LPA standard features of hierarchical processing, partitioning pattern filtering and distributed processing have been tuned for the integration with ASML Brion to deliver faster runtime.

Figure 3 shows a flow chart detailing the data flow through the LPA PLUS system.

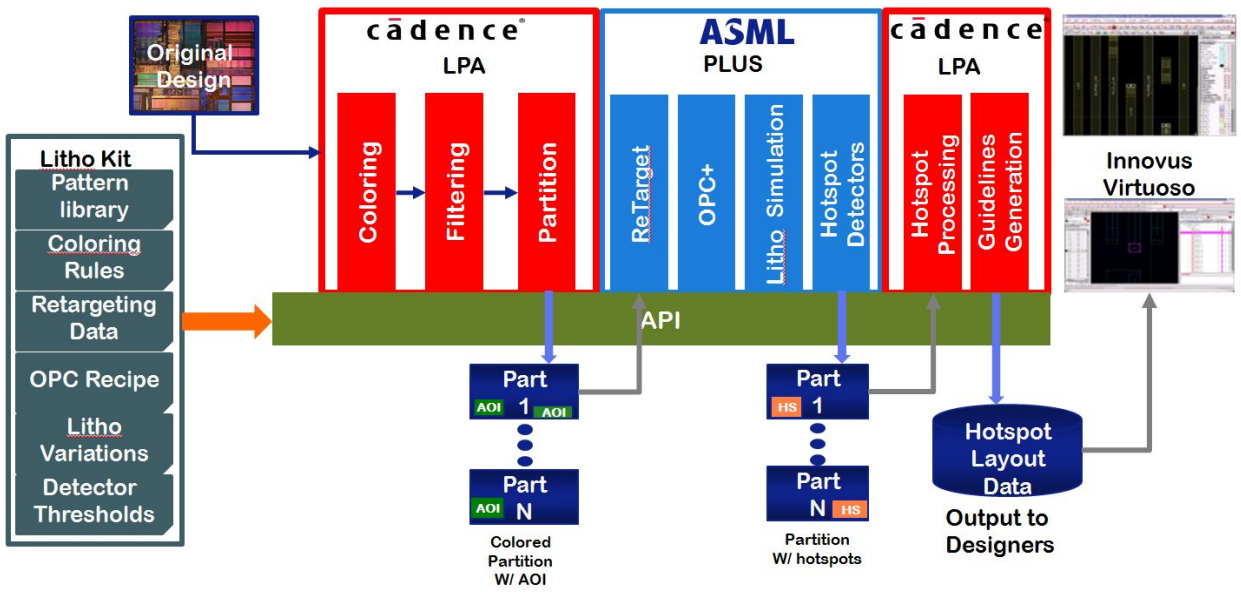

Figure 3. Flow chart for data processing from design environment through OPC and return of hotspots for repair and review.

3. IMEC 7NM EUV OPC AND HOTSPOT DETECTOR RECIPES

In the IMEC iN7 node there is active research ongoing to the patterning strategy that best fits the requirements of the design and process technology. Single patterning EUV and a self aligned quad patterning (SAQP) with DUV mandrel and EUV cut are in consideration for the metal interconnect layers. Innovus place and route test designs were studied with these two options and the parasitic capacitances and power estimates where generated to guide the patterning technology decision. It is well known that the self aligned multi patterning can add significant parasitic capacitance from the required line end extensions and dummy wires added to accommodate cut mask constraints. The layout reasoning along with the place and route wire length, parasitic capacitance and final power estimation for the two options is presented in Figure 4. Based on this result the single patterning EUV solution was selected for M1 and the SAQP solution was selected for M2. The RET and SMO optimized sources used in this case study are presented in Figure 5.

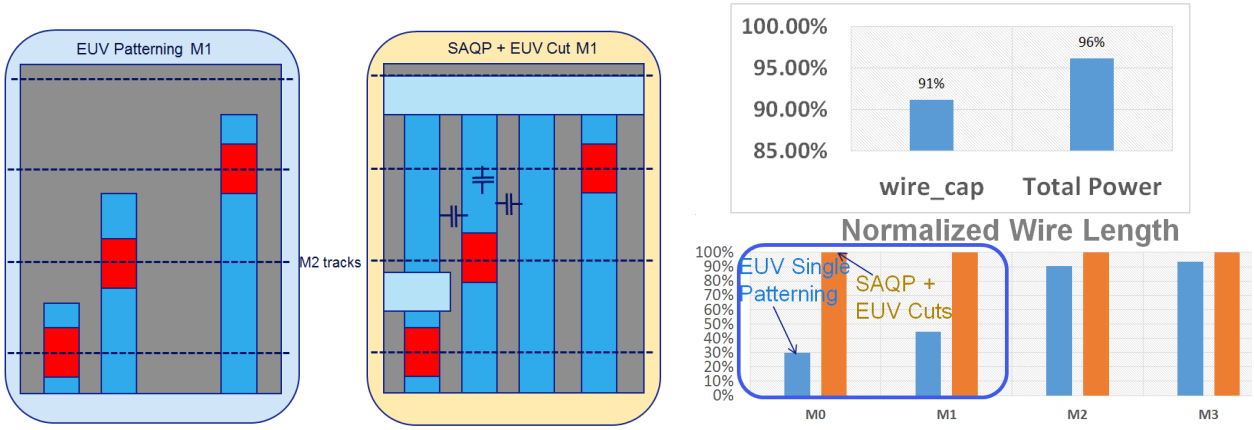

Figure 4. Parasitic estimation for the EUV single patterning vs SAQP shows dramatic wire length and power reduction for direct print on M0/M1, but less impact on M2 and above.

The “7nm” node from IMEC interconnect flow was developed using EUV lithography for metal1 and via1 and a self aligned quad patterning with DUV mandrel and EUV cuts was developed based on Tachyon OPC+ and LMC. This

recipe was then incorporated into LPA PLUS. Figure 4 details the sources, minimum dimension and pitch, and typical logic layout for each the layers going into the printability analysis.

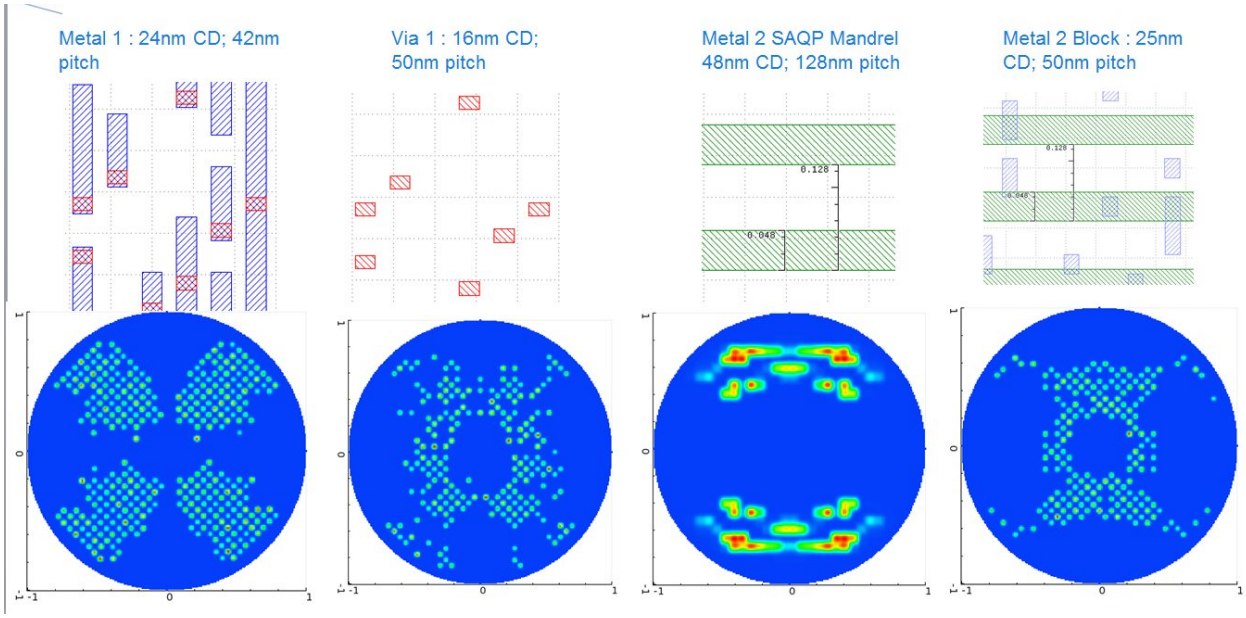

Figure 5. Details of CD and pitches for the 7nm logical layout used for print image analysis

4. MANAGING FLARE VARIATION IN DFM

Flare variation and correction is a critical part of the final CD control for EUV. In the DFM context it is critical that the evaluation of candidate layouts for a product be vetted against the range of possible flare environments where the design may occur and ensure that the manufacturability analysis done at the cell level ensures success in the production context. This requires either knowledge of the final use environment or guard banding to be added into the DFM flow. For this study we have produced some example flare maps and used the worst case flare for the DFM simulations. An example flare map is shown in Figure 6 with the worst case flare of ~2.5% transferred into the DFM setup recipes. The flare value depends on the scanner lens point spread function convoluted with the design density. This means the final flare map will depend on the design but typical density ranges and worst case values can be easily incorporated into the DFM recipe by the foundry.

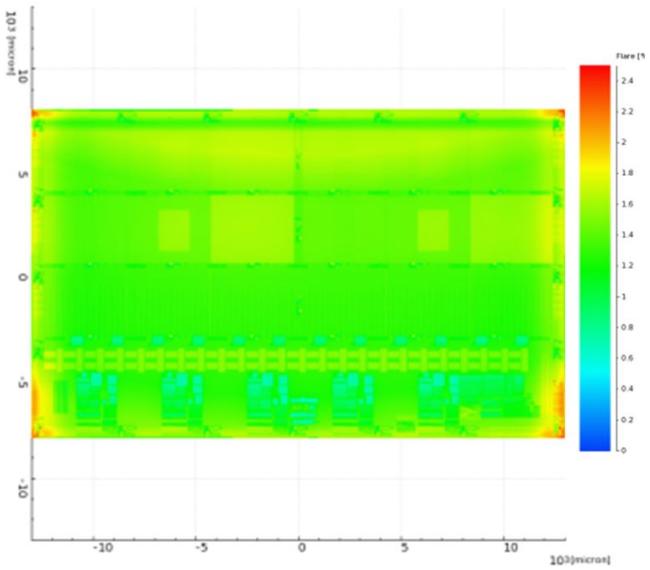

Figure 6. Typical flare map indicating worst case flare occurs at field corner; ~2.5% used for DFM simulations.

5. IMPROVING TURNAROUND TIME IN FABLESS DESIGN

Complete sign off OPC and printability verification across multiple process window corners is slow compared to typical design verification operations like DRC/LVS. Despite the cost, additional value comes from the accuracy and any potential risky layout patterns that would not be detected by normal design verification. Still additional runtime improvement options are integrated into the LPA PLUS product which can maintain the additional risk reduction while improving cycle time.

Several runtime reduction approaches exist. Core count scaling is of course valuable and if the design area is large; it is helpful to have the patch count approximately equal to the core count so that the total cycle time can be maintained close to the cycle time for a single patch. For the EUV case the patch sizes were ~5um and for DUV the patch sizes are in the 7-15um range. This means that large designs will not be able to match this goal of patch count ~core count. To reduce cycle time for large designs filtering the design and reducing the area passed into print image flow can be used to save time. First known risky layout can be identified with CPA (Cadence pattern analysis) based on a library of potential yield detractor patterns[4] and this can dramatically reduce the required simulation area.

For the IMEC iN7 case several test designs were developed. We targeted small, medium, and large blocks that would represent the typical use models of an early development phase. In that case, there is not a pattern library yet to filter the design and 100% simulation area was used. Table 1 below describes the runtime for the 6 test layouts developed. The runtime goals were captured as “over coffee” for the small layouts, “over lunch” for medium layout, and “over night” for the large layout. These runtime goals are critical to design use models to enable fast iteration and provides a system that allows development iterations and ensures that physical designs can be validated quickly. For the small layout case the core count matches the patch count and the runtime goal is achieved. For the medium and large case the runtime is slightly over the goal but the value of production sign of verification justifies the cost and core count increases beyond the modest 64 core system used for this test would enable the development success.

Table 1. Runtime results for LPA PLUS testing based on IMEC iN7 EUV lithography for M1/V1/M2.

Design	Area (mm2)	# Instances	Instance per area (M/mm2)	Cores	Runtime (min)
Tiny	0.0004	4k	10.5	16	11
Small1	0.0009	9k	10.1	32	12
Small2	0.0008	9k	11.5	32	12
Medium1	0.02	148k	7.6	64	131
Medium2	0.02	149k	7.7	64	134
Large	0.16	1.7M	10.5	64	1048 (17 hrs)

CONCLUSION

ASML and Cadence have formed a new partnership for patterning and design development. Managing proximity and lithography effects are critical to meeting design technology co-optimization (DTCO) development cycle time and cost/performance goals for leading edge IC technology. LPA PLUS is an easy button for production hotspot detection with ASML Tachyon and enables DTCO and DFM/sign off checking. Runtime management using filtering and scalability to high core counts enables LPA PLUS sign off for IP development and large design projects. Finally, EUV specific patterning effects incorporated into hotspot management; enabling design/process co-optimization for EUV productization.

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