Future of Multiple-E-Beam Direct-Write Systems

Burn J. Lin*
Taiwan Semiconductor Manufacturing company, Ltd.
168 Park Ave. 2, Hsinchu Science Park, Hsinchu County, Taiwan 308-44 R.O.C.

ABSTRACT

The crossover of high-speed digital electronics, MEMS, and cost reduction presents an exciting opportunity to extend optical lithography with multiple e-beam direct write systems. Massive parallelism overcomes the throughput limitation of e-beam direct write systems. Many innovative concepts on multiple e-beam imaging have been conceived and are being developed for various applications, such as maskwriting, prototyping, writing critical layers in high volume manufacturing (HVM), and writing all layers in HVM. MEB DW systems are capable to do all of the above. For maskwriting, the writing time can be saved by between a factor of 5 and 10 but it takes similar efforts to develop the maskwriting technology as direct wafer writing. There is insufficient demand for maskwriting and prototyping tools to warrant the development efforts. Writing critical layers in HVM makes economic sense for wafer production and makes economic sense to develop the imaging tool. However, using MEB DW for critical and non-critical layers, especially for 450-mm wafers, presents a unique opportunity to save lithography cost for the 450-mm wafer technology. This is the most desirable application for MEB DW. Once this application is established, all other applications easily follow.

Keywords: e-beam lithography, maskless lithography, multiple e-beam direct write lithography, multiple e-beam maskless lithography, lithography cost reduction, massive parallelism.

1. INTRODUCTION

E-beam lithography has been popular in the 70s. Its dynamic writing capability was fully taken advantage to expose wafers and masks. Even reduction projection of the mask image has been demonstrated in that era[1]. At the direct writing side, serious efforts were made to fabricate 1-μm devices[2]. In order to eliminate the large number of masks needed for metal interconnects, e-beam direct write was used in manufacturing to write the metal and via layers[3]. People also took advantage of the high defection rate of e-beam to replace optical pattern generators[4]. E-beam lithography soon found a niche in mask making and has been used dominantly to make masks. However, direct writing on wafer gave way to optical lithography using massively parallel photons to reduce costs at the pace of Moore's Law. Therefore, e-beam direct writing on wafer has retracted to small scale writing of exploratory devices or prototyping. It is very popular in the academic laboratories to write small fields, because of the freedom from making masks for cost and cycle time.

Recently, optical lithography has exhausted its resolution potentials in wavelength reduction, NA increase, mask/illumination optimization, and proximity correction. The attempt to further reduce wavelength to the 13.5-nm extreme UV (EUV) regime is not yet materialized. The industry has been reluctantly using multiple exposures with the exhausted optical resolution to uphold Moore's law. Cost is escalated. New restrictions have to be added to the design rules. On the other hand, with the advent of MEMS fabrication technology, the high speed and high capacity electronics resulting from the advent of Moore's Law, begins to make massively parallel e-beam direct write appealing in cost and extendibility. There is likelihood that Moore's Law is now helping MEB to uphold Moore's Law. Even though EUV is still under development, the development of EUV resist systems greatly reduces the efforts to develop e-beam resist systems, because EUV resist exposure is due to the secondary electrons generated by the high energy photon. For lack of EUV exposure tools for resist system development, most resist suppliers use e-beam exposure to screen their EUV resists anyway.

* burnlin@tsmc.com; phone +886-3-563-6688 ext 722-5858; fax +886-3-578-7737.

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There are attempts to take advantage of the much higher throughput enabled by multiple e-beam technology to speed up maskwriting and prototyping[5,6]. There are also efforts to develop systems capable of high volume manufacturing (HVM) of the most critical layers that have exhausted the economical imaging capability of optical lithography to mix with layers that can be economically exposed with optical lithography. Ultimately, if cost allows, MEB DW systems can be used in HVM for all layers. In this presentation, we make a comparison of these four applications and point out the most likely applications to succeed.

2. MASKWRITING WITH MEB LITHOGRAPHY

With a single e-beam, mask making is now under the pressure of Moore's Law to deliver an ever increasing pixel count on the same writing area on the mask. The writing time for the most recent advanced nodes can be days. With MEB, that writing time can reduce to hours[5]. This is a very strong impetus to apply MEB DW to maskwriting.

However, several aspects have to be considered. First, even at 4X, maskwriting is more stringent than wafer writing. As seen in Table 1, for 10-nm holes and 10-nm lines, the same corresponding feature on the mask is four times larger. This should make it easier. However, because of assist features and other small variations required of optical proximity correction (OPC), source/mask optimization, or inverse lithography; the minimum feature to delineate on the mask is actually also 10 nm instead of 40. The wafer CD tolerance is typically 10% of CD. On the mask, only 0.6 of the wafer CD tolerance is given to the mask CD tolerance. This tolerance has to be tightened by the mask error enhancement factor (MEEF) incurred from low-k_1 diffraction and the writing error enhancement factor[7] (WEEF) incurred from e-beam writing. The CD tolerance is 10*6%/4/2=0.075 nm for the 40-nm hole on the mask. It is much tighter than the 0.5-nm CD tolerance for 10-nm holes on the wafer. Similarly, the CD tolerance required of the 40-nm line on the mask is much tighter than the 0.77-nm tolerance on the wafer. In reality, the requirement of assist features and the like on the mask may not have to be as stringent as the main features. Therefore, it is relaxed to 12% instead of 6%. The resulting mask CD tolerance, 0.15 and 0.46 nm, for holes and lines respectively, is still tighter than that for wafer imaging. Even with CD tolerance on mask relaxed further to 18%, the resultant 0.23 and 0.69 nm mask CD tolerance requirement is still tighter than that of wafer imaging. These tolerances were established without considering OPC errors. When the latter are incorporated, the requirement on the mask may be physically impossible.

	Mask writer		Wafer writer	
	Hole	Line	Hole	Line
CD (nm) to write	40	40	10	10
Reduction ratio	4	4	1	1
Min. Feature (nm) to write	10	10	10	10
CD tol required	6%	6%	10%	10%
MEEF	4	2	1	1
WEEF	2	1.3	2	1.3
Overall CDU requirement without OPC error (nm)	0.08	0.23	0.50	0.77
CDU requirement after allowing 2X tol. for assist features (nm)	0.15	0.46	NA	NA
CDU requirement after allowing 3X tol. for assist features (nm)	0.23	0.69	NA	NA

Table 1 CDU requirements on mask and wafer writings.

In addition to impossibly tight CD control on the mask, a fast maskwriter is self destructive businesswise. The number of single-beam maskwriters is barely sufficient to sustain the business. With a faster writer, the number of writers needed is even smaller, making this type of tool unsustainable. In addition to sustaining, the development cost of a MEB DW maskwriter is no less than that of a wafer writer. A plausible way to provide the industry with a fast maskwriter is to leverage the development of a fast wafer writer suitable for HVM.

3. PROTOTYPING WITH MEB DW

A direct writing tool can be used for prototyping to prove out a given design in order to avoid the mask cost and to eliminate the time needed for maskmaking. It can also be used to run small lots for the same purposes.

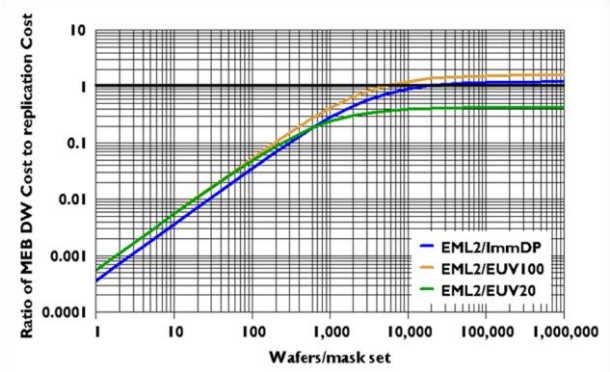

Fig. 1 Crossover points in cost of direct writing vs. mask making + replication as a function of number of wafers replicated per mask set.

Prototyping with MEB DW is not feasible, if the HVM of the main lot does not use MEB DW, because the process used for prototyping and HVM should be identical.

Using MEB DW only for small lots puts little demand of the tool, so that the size of the demand does not warrant the development cost of the MEB DW tool and cannot sustain the business. We made[8] an estimate of the cost crossover point between MEB DW and replication, as shown in Fig. 1. EML2 represents e-beam maskless lithography; ImmDP, immersion double patterning; EUV100, EUV tool at €50M and 100 wph; EUV20, EUV tool at the same cost but 20 wph. The crossover points are the intersection of the unity cost-ratio line. They are listed in Table 2. For EUV100, the crossover point is 5,048 wafers per mask set; and for double patterning on an immersion scanner, 18,718 wafers. Two immersion masks were estimated to cost $20K and one EUV mask, $13K. The crossover point for the EUV20 system is infinity, meaning that the exposure + material cost per exposure from EUV20 is higher than that with MEB DW, regardless of the number of wafers that each mask is replicated to. Table 2 also shows that the MEB DW tool at 20 wph can be priced at €13.33M to put the crossover point with EUV100 at infinity. The price for a 40-wph MEB tool can be €70M to be equivalent to EUV20. However, there is no reason MEB DW tools will cost that much. Even with crossover point at 5000 wafers/mask and the tremendous wafer volume of TSMC, the number of prototyping tools needed is in the single digit, hardly sufficient to interest potential equipment suppliers. In addition to the small number of tools, it is not economical to implement two tool sets for small lots and HVM. Two different sets of tool have to be installed. Two types of equipment, processing, and maintenance experts have to be employed and trained. Not to mention that much more floor space has to be allocated. The cost saving in masks can be alleviated with the mask-sharing program provided by most semiconductor foundries.

	H_2O Imm DP	EUV 50M/100	EUV 50M/20
MEB 20M/20 Crossover no. wafers / mask	18,718	5,048	∞
MEB Price at 20 wph for same expo+mat /layer cost (M€)	17.23	13.33	43.67
MEB Price at 40 wph for same expo+mat /layer cost (M€)	27.65	21.39	70.07

Table 2 Tool price and crossover.

4. MEB DW EXPOSING CRITICAL LAYERS

Most recent developments of MEB DW systems are geared towards exposing the most critical layers in a given technology. We just assume that existing technology to expose the less critical layers will continue to be used with the tools chosen for HVM of the critical layers. For this purpose, several tools are viable candidates.

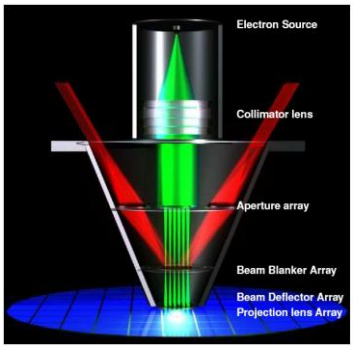

Fig. 2 MAPPER e-beam column.

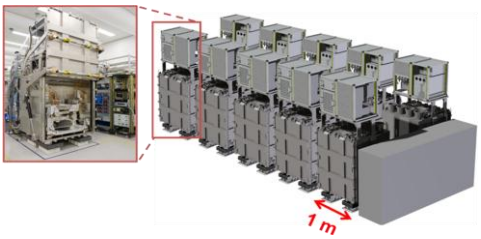

Fig. 3 MAPPER cluster.

The Multiple Aperture Pixel by Pixel Enhancement of Resolution (MAPPER) 5-keV system shown in Fig. 2 has been widely reported[9, 10, 11]. It employs a unique combination of MEMS and MEB technology to offer a compact 10-wph column. A single source with a collimator provides a uniform beam to be broken into 13K Gaussian beams, each of which is further subdivided to 49 subbeams using a patterned beam concept. Fiber optics carries the switching information to be detected by photodiodes and amplified by CMOS circuits on the beam blanker array. The beams are deflected and projected to the wafer. With the clustering scheme shown in Fig. 3, the system is capable for HVM with 100-wph throughput with the footprint assimilating that of an immersion scanner. Experimental results substantiated many of the MAPPER performance claims[12,13]. A DOF experiment evaluating the CD variation in 11 randomly picked beams from a total of 110 beams confirms that the DOF is easily 1 μm as shown in Fig. 4.

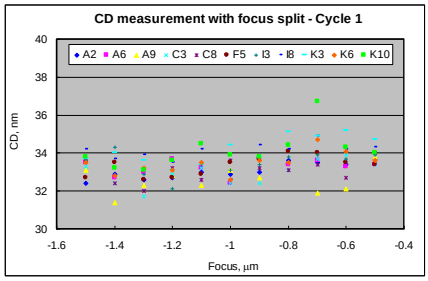

Fig. 4 DOF of the MAPPER pre-α tool.

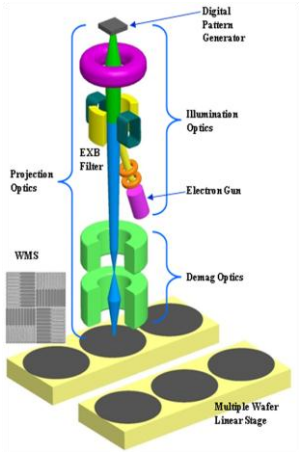

Fig. 5 The REBL system.

The Reflective E-Beam Lithography (REBL) tool[14,15] from KLA-Tencor consists of reflective electron optics, dynamic pattern generator (DPG), temporal dose integration, optical wafer alignment, and MAGLEV stage technology as shown in Fig. 5. The illumination beam from the obliquely oriented electron gun is bent to incident on the DPG at a normal angle and is decelerated to a very low voltage. The DPG is a CMOS circuit with its last layer of metal pads facing the low-voltage illumination. The pads with a negative voltage in the order of 2 volts reflect the electrons back through the reduction imaging electron optics to expose the wafer. The pads that have a negligible voltage absorb the incident electrons. The electro optics column of the REBL system is designed to eventually be 10 cm in diameter for the HVM system. Such a small diameter facilitates clustering of columns on the wafer as shown in Fig. 6. As many as 36 columns can be clustered on either the rotary or the new linear stage using 300-mm wafers. The REBL system may use 50 or 100 keV acceleration voltage. The Exposure-Defocus (E-D) window of a 100-keV system for isolated and dense holes and line/space has been simulated as shown in Fig. 7. Resist scattering of the e-beam and a 10-μm blur by acid diffusion are included in the simulation. The resist thickness for the holes is 65 nm and that for the line/space is 50 nm. The half pitch (HP) chosen for the holes is 21 nm and that for the line/space is 15 nm. The DOF of holes is 1.3 μm at 15% exposure latitude; and that for the line/space, 1 μm at 10% EL.

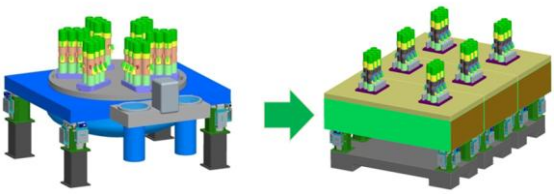

Fig. 6 Rotary new linear stages for REBL HVM.

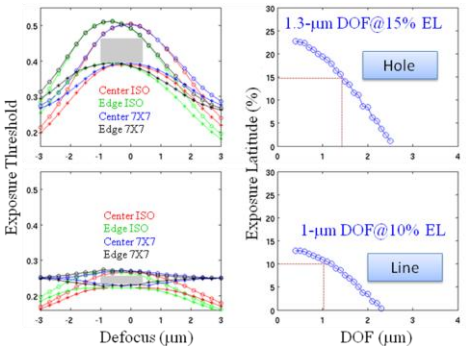

Fig. 7 Elat and DOF of 100 keV beam at1.5 μA to support 75 wph at the 10nm node.

The IMS PML MEB DW system[16] shown in Fig. 8 uses a reduction projection scheme similar to that of REBL. It also has a programmable mask except that it transmits instead of reflects. The blanking and deflection scheme is similar to that of MAPPER. Impressive images have been demonstrated as seen in Fig. 9, showing HP as small as 16 nm.

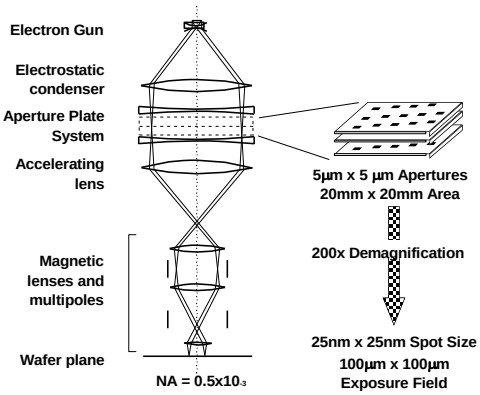

Fig. 8 50-keV MEB DW system from IMS.

All these three systems show potential for high resolution and high throughput MEB DW imaging for HVM. All still need much development work for HVM.

We would like to set a realistic dosage by considering the shot noise limit.

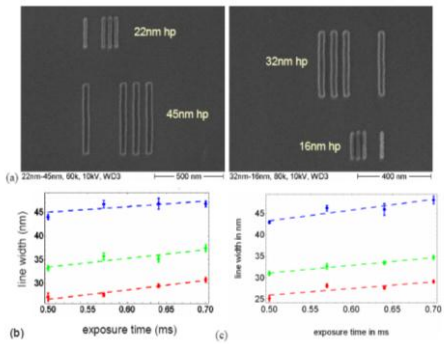

Fig. 9 Resolution of IMS PML2 tool at 50 keV.

The effect of shot noise is multifold. It can cause CD variation, line edge or line width roughness (LER/LWR), and placement error in the resist image resulting in overlay errors and beam position measurement error. We maintain that 60 μC/cm^2 containing ~1500 electrons in 20x20 nm^2 is sufficient for up to the 10-nm node and that there is opportunity to reduce the number of electrons further. The distribution of these 1500 electrons is depicted in Fig. 10. Experimental results[7] from the MAPPER pre-α tool depicted in Fig. 11 shows inconsistency of CD non-uniformity to the change of exposure dosage among

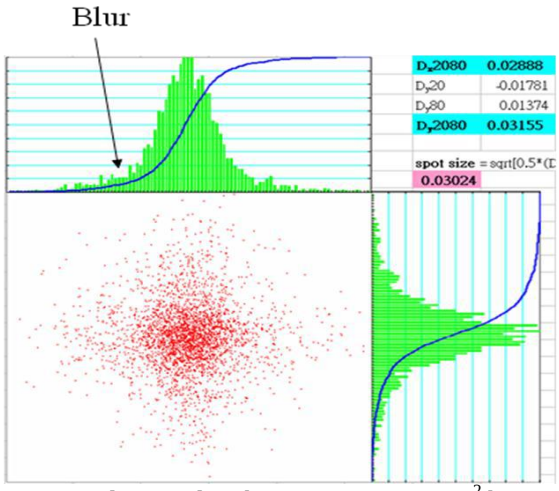

Fig. 10 Electron distribution in a 20x20 nm^2 beam

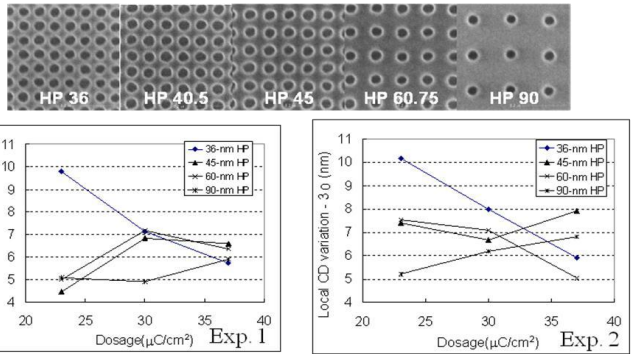

Fig. 11 CD 3σ vs. exposure dosage.

different pitches but from the same CD, suggesting that even between 20 and 35 μC/cm^2, the shot noise is not dominating in CD variation.

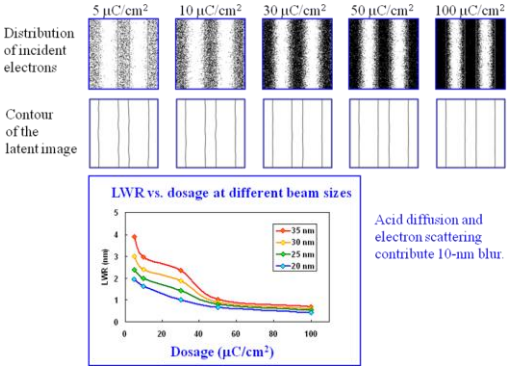

Fig. 12 LWR vs. exposure dosage.

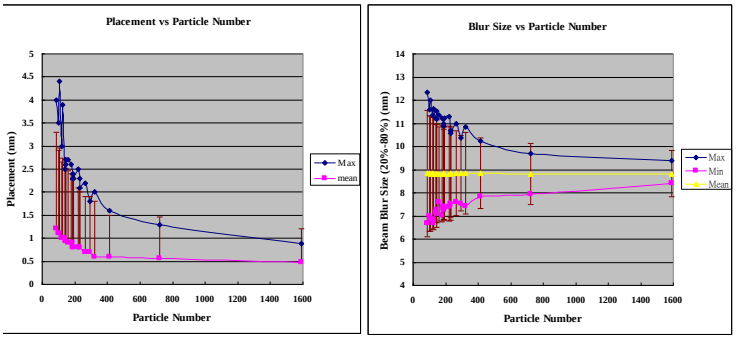

Fig. 13 Shot noise induced placement errors.

The LWR of 20- to 35-nm lines is simulated for dosage between 5 and 100 μC/cm^2. It is seen[17] in Fig. 12 that the LWR drops to below 1 nm for all feature sizes as long as the dosage is above 50 μC/cm^2 and stays practically constant with larger dosages. Therefore, using 60 μC/cm^2 is a safe assumption.

To study the placement error induced by shot noise, Monte Carlo simulation through the REBL electro optics was performed using 100-keV acceleration voltage and 1.5-μA beam current. The placement error and blur size as functions of the number of electrons are plotted as shown in Fig. 13. After the number of electrons reached 1300, corresponding to less than 60 μC/cm^2, the placement error reduces to below 1 nm and the blur size variation is within ±1 nm.

5. MEB DW EXPOSING ALL LAYERS FOR ALL WAFER SIZES

MEB DW systems have a cost advantage over EUV or ArF immersion scanners for critical layer patterning as seen in Sec. 3. They also have a cost advantage over scanners of similar imaging performance for non-critical layers. For larger features, a larger blur size is allowed thus permitting a higher beam current to expose the wafer. In addition, resists of higher sensitivity can be used because the shot noise effect is less severe for larger features. Since each column supports more wph, the number of e-beam columns and platforms can be reduced and thus, cost is reduced. The cost of datapath also reduces accordingly.

We calculated the cost for earlier technology nodes to represent the cost associated with less critical layers. The result is presented here. Table 3 shows the assumption we made for the calculation. The spot size required to delineate the minimum features is normalized to that for the 10-nm node. Physically, it is slightly larger than 1 nm. The requirement of such a blur size puts a limit on the beam current through the electro optics column. Exceeding it, the space charge effect will cause aberrations. The blur-limited beam current was obtained by careful simulation of beam current through

Node (nm)	180	130	90	65	40	28	20	14	10
Spot(blur) size with 3.5 NILS normalized to 10nm node	17.3	12.1	8.5	5.9	4.2	2.9	2.0	1.4	1.0
Blur-limited beam current / col. normalized to 10nm node	49.3	33.9	23.1	15.6	10.3	6.7	4.1	2.3	1.0
Beam current reduction ratio per node		0.7	0.7	0.7	0.7	0.6	0.6	0.6	0.4
Throughput loss from stitching (TSMC estimate)	6.1%	6.1%	6.1%	6.1%	6.1%	6.1%	6.1%	6.1%	6.1%
Throughput loss from overhead (TSMC estimate)	2.78%	2.78%	2.78%	2.78%	2.78%	2.78%	2.78%	2.78%	2.78%
Throughput loss from wasted area (geometrical)	31.5%	31.5%	31.5%	31.5%	31.5%	31.5%	31.5%	31.5%	31.5%
Resist sensitivity ($\mu C/cm^2$)	20	20	20	20	40	40	40	60	60

Table 3 Assumption for all-layer REBL system.

the column design parameters. It turns out that the beam current reduction ratio is 0.7 from one node to the other, for the less critical layers. It then reduces more rapidly through the more critical layers. The throughput calculated from the beam current has to be corrected for losses from pattern stitching, scanning overheads, and wasted Si coverage due to round wafers. The resist sensitivity is assumed to be higher for the less critical layers because of less shot noise effect from more electrons in larger features since the CDU, LWR, and placement are less stringent.

With these assumptions, we then calculate the throughput of holes and line/space patterns for 300-mm and 450-mm wafers based on the cost of columns, platforms, infrastructure, common and dedicated datapaths. Table 4 shows the throughput and cost of hole patterns with 6% pattern density. The required beam current on DPG is the incident current on the DPG that will supply the blur-limited current through the electro optics. It is simply the blur-limited current divided by the pattern density. This incident current on the DPG cannot be increased at will for the less critical layers, because of the brightness limit from the illumination source. Here, the limit is 102.1 normalized to the blur-limited current. The available current per column on wafer is the brightness limited beam current on DPG multiplied by the pattern density. This is the current that exposes the resist on the wafer. Based on this current, the assumed resist sensitivity, and the total wafer area less the throughput loss by stitching, overhead, and non-Si wasted area, the throughput per column is calculated. Then, the number of platforms and the number of columns in the platform, are arranged to produce approximately 150 wph per tool. The tool cost is then calculated based on the unit cost of electro optic columns, platforms, infrastructure, common and column-dedicated datapaths, then normalized to the tool cost of an EUV scanner capable for the 14-nm node at the manufacturer's specified throughput. The normalized tool cost per wph is just the normalized tool cost divided by the wph of the tool and the normalized Si per area per wph cost is the normalized tool cost per wph further divided by the wafer area. The contact hole layer is extremely favorable for MEB DW because of the low pattern density. The tool cost for the 10-nm node is only 72% of that of EUV scanner for the 14-nm node. Comparing 14 nm MEB to 14 nm EUV, the saving is an astonishing 35%. Needless to say, the Si/area/wph cost is also lower even from 10-nm MEB to 14-nm EUV.

Node (nm)		180	130	90	65	40	28	20	14	10
Holes pattern density		6%	6%	6%	6%	6%	6%	6%	6%	6%
Required beam current / col. on DPG with respect to 10nm blur-limited beam current		821.3	565.1	385.8	260.3	172.5	111.0	67.9	37.8	16.7
Beam current on DPG not exceeding source brightness limit per col. with respect to 10nm blur-limited beam current		102.1	102.1	102.1	102.1	102.1	102.1	67.9	37.8	16.7
Avail. beam current/col. on wafer for Holes, with respect to 10nm beam current on DPG		6.12	6.12	6.12	6.12	6.12	6.12	4.07	2.27	1.00
Hole CD (nm)		364	255	178	125	87	61	43	30	21
Pixel size for hole (nm) - 1/4 of CD		91.1	63.7	44.6	31.2	21.9	15.3	10.7	7.5	5.3
Grey level		5	5	5	5	5	5	5	5	5
Data rate/column(Gbps) for holes		21.7	44.3	90.4	184	188	384	522	395	355
Hardware	wph / column	21.6	21.6	21.6	21.6	10.8	10.8	7.2	2.7	1.2
	No. of Columns	7	7	7	7	14	14	21	28	36
	No. of Platforms	1	1	1	1	1	1	1	2	4
	Total wph	151.1	151	151	151	151	151	151	149	169
Costs include platforms, columns, datapath, & infrastructure normalized to 14nm EUV	Tool cost normalized to EUV14	8%	9%	9%	10%	12%	14%	19%	35%	72%
	Normalized tool cost / wph	5.5E-04	5.6E-04	5.9E-04	6.5E-04	8.1E-04	9.6E-04	1.3E-03	2.4E-03	4.3E-03
	Normalized Si cost / ($wph*cm^2$)	7.8E-07	8.0E-07	8.4E-07	9.2E-07	1.2E-06	1.4E-06	1.8E-06	3.4E-06	6.0E-06

Table 4 REBL cost and throughput for holes on 300-mm wafers with respect to EUV scanner for 14-nm node.

The cost and throughput of line/space patterns, are shown in Table 5. The difference to the hole patterns is in the 20% pattern density. With special data handling, we do not have to go beyond 20% for any given layout. Even so, the higher pattern density reduces throughput. The throughput per column now drops to 0.4 wph instead of 1.2 as in the case of 6% hole pattern density. Except for the 10-nm node, we still design the system to produce more than 100 wph. In many cases, the cost is more favorable by arranging the number of columns and platforms to reach about 200 wph. Comparing with a 14-nm node EUV scanner, the cost of 14-nm node REBL tool for line/space is 79%, not as impressive as 35% but is still less expensive. In terms of Si/area/wph cost, REBL is higher by about 3% at the 14 nm node for line/space.

Node (nm)		180	130	90	65	40	28	20	14	10
LS pattern density		20%	20%	20%	20%	20%	20%	20%	20%	20%
Required beam current / col. on DPG with respect to 10nm blur-limited beam current		246.4	169.5	115.7	78.1	51.7	33.3	20.4	11.3	5.0
Beam current on DPG not exceeding source brightness limit per col. with respect to 10nm blur-limited beam current		102.1	102.1	102.1	78.1	51.7	33.3	20.4	11.3	5.0
Avail. beam current/col. on wafer for L/S, with respect to 10nm beam current on DPG		20.4	20.4	20.4	15.6	10.3	6.7	4.1	2.3	1.0
LS CD (nm)		180	130	90	65	40	28	20	14	10
Data rate/column(Gbps) for L/S		296	568	1185	1738	1521	1996	2395	1812	1567
Hardware	wph/column	18.4	21.6	21.6	16.5	5.5	3.5	2.2	0.8	0.4
	No. of Columns	9	9	9	12	36	36	36	36	36
	No. of Platforms	1	1	1	1	1	1	2	4	6
	Total wph	165	194	194	198	197	127	155	115	76
Cost: Includes platforms, columns, datapath, and infrastructure (normalized to 14nm EUV)	Tool cost normalized to EUV14	9%	10%	11%	14%	22%	24%	45%	79%	106%
	Normalized tool cost / wph	5.6E-04	5.1E-04	5.8E-04	6.9E-04	1.1E-03	1.9E-03	2.9E-03	6.8E-03	1.4E-02
	Normalized Si cost / (wph*cm^2)	8.0E-07	7.2E-07	8.2E-07	9.7E-07	1.6E-06	2.7E-06	4.1E-06	9.7E-06	2.0E-05

Table 5 REBL cost and throughput for line/space on 300-mm wafers with respect to EUV scanner for 14-nm node.

Since the pattern density of each layer is different, we need to use an average throughput to calculate the Si/area/wph cost for fair comparison. The result is shown in Table 6. Here, the tool cost and Si/area/wph are both very favorable for REBL.

L/S and Hole Average cost (normalized)	Avg throughput (wph)	158	170	170	172	171	138	153	130	105
	Normalized L/S-Hole avg cost	9%	9%	10%	12%	17%	19%	32%	57%	89%
	Normalized Avg cost / wph	5.6E-04	5.4E-04	5.9E-04	6.7E-04	9.7E-04	1.4E-03	2.1E-03	4.6E-03	9.1E-03
	Normalized Avg cost/(wph-cm^2)	7.9E-07	7.6E-07	8.3E-07	9.5E-07	1.4E-06	2.0E-06	2.9E-06	6.5E-06	1.3E-05

Table 6 Average REBL throughput and cost on 300-mm wafers with respect to EUV scanner for 14-nm node..

For 450-mm wafers, the considerations are similar. As a result, the beam currents per column, CD, pixel size, number of gray level, and data rate per column are identical to those for 300-mm wafers. Therefore, only the system configuration, costs, and throughput are shown in Table 7. Here, the tool cost is higher than its 350-mm counterparts. However the Si/area/wph cost is lower than the 350-mm counterpart in all categories thus, much more economical than 14-nm EUV scanner. The reason that the REBL system is more economical for larger size wafers can be seen in Fig. 14. In this case the rotary stage is used for demonstration. Eight 300-mm wafers are placed at the rotary stage. This allows placement of 36 electro optics columns on the wafers. On the 450-mm wafer stage, 81 columns can be placed on the eight wafers. Unlike optical columns with high-NA and high-precision optics, these electro columns are much less expensive to make. Placing more columns on each platform makes the system more productive, thus more economical.

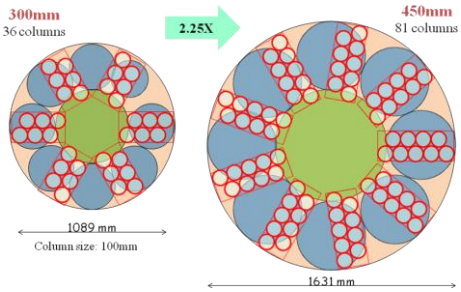

Fig. 14 More e-beam columns on 450-mm wafer.

Node (nm)		130	90	65	40	28	20	14	10
Hardware	wph / column	9.6	9.6	9.6	4.8	4.8	3.2	1.2	0.5
	No. of Columns	22	22	22	43	43	64	81	81
	No. of Platforms	1	1	1	1	1	1	2	3
	Total wph	211	211	211	206	206	204	192	127
Cost: Includes platforms, columns, datapath, and infrastructure (normalized to	Tool cost normalized to EUV14	13%	14%	15%	22%	26%	38%	78%	104%
	Normalized tool cost / wph	6.2E-04	6.5E-04	7.1E-04	1.1E-03	1.3E-03	1.8E-03	4.1E-03	8.2E-03
	Normalized Si cost / (wph*cm^2)	3.9E-07	4.1E-07	4.5E-07	6.8E-07	7.9E-07	1.2E-06	2.6E-06	5.2E-06

Line/Space pattern density		20%	20%	20%	20%	20%	20%	20%	20%
Hardware	wph/column	9.6	9.6	7.3	2.4	1.6	1.0	0.4	0.2
	No. of Columns	20	20	28	81	81	81	81	81
	No. of Platforms	1	1	1	1	1	1	3	4
	Total wph	192	192	206	197	127	78	86	51
Cost: Includes platforms, columns, datapath, and infrastructure (normalized to	Tool cost normalized to EUV14	14%	15%	20%	40%	43%	45%	114%	137%
	Normalized tool cost / wph	7.1E-04	8.0E-04	9.7E-04	2.0E-03	3.4E-03	5.8E-03	1.3E-02	2.7E-02
	Normalized Si cost / (wph*cm^2)	4.4E-07	5.0E-07	6.1E-07	1.3E-06	2.1E-06	3.6E-06	8.3E-06	1.7E-05

Average cost (normalized)	Avg throughput (wph)	201	201	208	202	157	112	119	73
	Normalized L/S-Hole avg cost	13%	15%	17%	31%	34%	41%	96%	120%
	Normalized Avg cost / wph	6.7E-04	7.2E-04	8.4E-04	1.5E-03	2.3E-03	3.8E-03	8.6E-03	1.8E-02
	Normalized Avg cost/(wph-cm^2)	4.2E-07	4.6E-07	5.3E-07	9.7E-07	1.5E-06	2.4E-06	5.4E-06	1.1E-05

Table 7 Average REBL throughput and cost on 450-mm wafers with respect to EUV scanner for 14-nm node.

From Tables 4 to 7, the cost of REBL and scanners are normalized to that of the 300-mm EUV scanner so that the relative cost of the scanners can be apprehended. But for a fair comparison, the cost of the less critical layers using REBL has to be compared with that of less advanced steppers such as ArF immersion scanner, and ArF dry scanner. Table provides such data. The normalization is now referring to the less expensive scanner that can handle the particular layer. For the 90- to 180-nm nodes, the reference is still to the ArF scanner, because KrF scanners cannot satisfy the overlay and DOF requirement for the implant layers of the advanced nodes. Table 8 shows that the REBL tool is less expensive than ArF dry scanner by between 30% and 40% for layers corresponding to the 180-nm to the 65-nm nodes. The REBL tool cost is only 35% of the cost of ArF scanners used for double patterning. It is 66% of an ideal EUV scanner suitable for delineating the 14-nm node. The cost of 450-mm MEB DW systems is even lower. For 450-mm wafers, the cost still refers to that of 300-mm scanners to show the relative improvement from 300- to 450-mm wafers. We do not expect large cost breakthrough from increase of wafer size with the scanners, because the size of scanner lens column does not facilitate mounting many more columns in the scanner even with a larger wafer. Also the lens column takes a much larger percentage of the tool cost than MEB DW columns.

Node (nm)		180	130	90	65	28	20	14
	Refering to	ArF dry	ArF dry	ArF dry	ArF dry	ArF Imm	ArF Imm	EUV
300mm L/S-Hole Average	Avg throughput (wph)	170	170	170	172	138	153	130
	Normalized avg tool cost	32%	33%	36%	42%	37%	53%	57%
	Norm. avg Si cost/(wph*cm^2)	30%	31%	34%	40%	53%	69%	66%
							35% for 2P	
450mm L/S-Hole Average	Avg throughput (wph)	201	201	201	208	157	112	119
	Normalized avg tool cost	46%	48%	52%	62%	65%	68%	96%
	Norm. avg Si cost/(wph*cm^2)	16%	17%	19%	22%	37%	54%	54%
							27% for 2P	
Impovement from 300 to 450 mm		55%	55%	54%	55%	69%	78%	82%

Table 8 300- & 450-mm REBL cost with respect to 300-mm ArF dry, immersion, and EUVL scanners.

Even though the cost is lower for MEB DW, there is concern on the portability of resists. Intuition favors scanners because the exposure wavelength does not change with wafer size. People may expect direct portability of resists from 300- to 450-mm wafers. However, during the transition from 200- to 300-mm wafers, the resist had to be modified to facilitate coating with a lower spin speed. Transitioning from 300- to 450-mm wafers would require at least this much

work on the resist. The need of resist modification and re-characterization presents a golden opportunity to switch to a better resist anyway.

For non-critical layers dealing mostly with ion implantation, the key parameter required of the resist is thickness. Three resists were exposed with 50 keV e-beam using image size between 123 and 148 nm as shown in Fig. 15. The resist thickness is 650 nm for the well implant layers and 150 nm for the source/drain implant layers.

Using the same high accuracy platform of the critical layers ensures high overlay accuracy that is currently badly needed for people who want to save cost by using scanners that do not overkill in resolution. Equipping 450-mm scanners with higher overlay accuracy further increases the Si/area/wph cost than that shown in Table 8. Regardless of cost, imaging over topography is becoming a severe challenge for imaging implantation layers. MEB DW tools have ample DOF to support imaging over topography as shown in Fig. 16. E-D trees of isolated and dense features at the center and the edge of the electro optics field are constructed from simulation results. The simulation is based on the requirement of implanting wells requiring a resist thickness in the order of 700 nm and feature size of 150 nm in 300-nm pitch. The beam current on wafer is 4 μA at 16 mrad, with 20-nm acid diffusion length and the resist blur as a function of the beam blur at the best focus. The E-D trees and the corresponding E-D window are shown in Fig. 16. The E-D window measures 26% in exposure latitude and 5.9 μm in DOF. It is more than sufficient for ion implantation. In a separate simulation for source/drain implant, the E-D window measures 25% in exposure latitude and 5.8 μm in DOF, with 150 nm resist thickness, 7 μA beam current at 16 mrad.

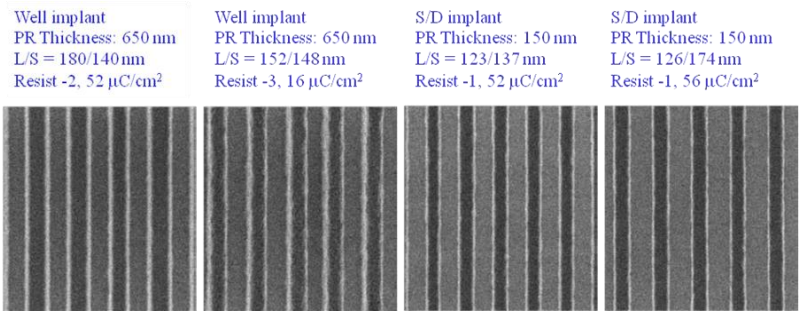

Fig. 15 Implant layers exposed by 100-keV e-beam. (Courtesy, Sumitomo Chemical Co., Ltd.)

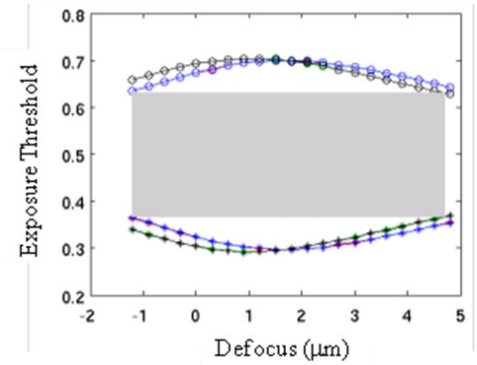

Fig. 16 E-D trees and E-D window for 14-nm node well implant.

After cost and resist portability, too much incident power on the wafer is another concern for MEB DW systems, especially for systems using 100 keV. The incident power and power density of the 100 keV system is compared to that of immersion and EUV scanners as shown in Table 9. Two extreme MEB DW cases are analyzed. For the line/space layer using conditions for the 130-nm node, 20 electro optic columns are used on the platform for 450-mm wafers. The maximum current is 20 μA. Hence, the power incident on the wafer is 40 watts distributed over the rotary platform which has a maximum diameter of 163 cm and a minimum diameter of 73 cm. The power density on the wafer is 2.4 mW/cm^2. The other exposure condition is line/space for the 10-nm node. With 81 columns at 1.2 μA, the incident power is 9.7 watts; and power density, 0.58 mW/cm^2. The power on wafer from immersion and EUV scanners are 1.39 and 0.625 mW/cm^2, respectively.

REBL							
Feature	No. Heads	μA	kV	Watt on wafers	Max. Disk Dia (cm)	Min Disk Dia. (cm)	W/cm^2 on wafer
Line/Space 130nm node	20	20	100	40.0	163	73	2.40E-03
Line/Space 10nm node	81	1.2	100	9.7	163	73	5.83E-04
Scanners							
	mJ/cm^2	wph		Watt on wafer		W/cm^2 on mask	W/cm^2 on wafer
Immersion	25	200		2.21		1.24E-04	1.39E-03
EUV	15	150		0.99		7.16E-04	6.25E-04

Table 9 100 keV E-beam, 193-nm and 13.5-nm incident power on wafer and mask.

Therefore, there are clear advantages using MEB DW for all layers, especially when switching over to 450-mm wafers. When the wafer size changed from 200 to 300 mm, lithography depended on the twin-scan innovation to maintain photon productivity to realize the cost saving in increasing the wafer size. A similarly effective innovation is needed for the 450-mm transition. To date, MEB DW is the only known innovation to realize lithography cost saving for increasing the wafer size to 450 mm.

In addition to cost, overlay accuracy, and DOF; MEB DW using the REBL writing strategy for all layers removes the 26x33 mm^2 field size limitation imposed by the mask and the scanner lens. It also simplifies matching between tools

used for different layers. The contribution of mask CDU and placement accuracy to the wafer CDU and overlay budgets can now be eliminated, resulting in more forgiving CDU and overlay accuracy requirement for the wafer.

All the problems induced by the mask are eliminated, namely mask cost, repair, inspection, contamination, and cycle time. However, more wafer inspection for MEB DW is needed to ensure removal of systematic errors. Many measures can be used to reduce this inspection. Data generation errors can be prevented with electronic data checking before outputting for writing. The platform concept to expose many wafers together, provides ample space to place monitoring and characterizing sensors for real time adjustment and correction during writing. Of course, exposure generated errors should be kept at the same level as those from scanners.

Not only the tool and exposure costs of MEB DW are cheaper for all layers. The development cost for REBL tool for 450-mm wafers consists of the development cost of only one common platform and one common column with minor finetuning optimizations. Whereas, EUV and UV platforms have to be developed for scanners. Four imaging wavelengths and the corresponding infrastructure for KrF dry, ArF dry, ArF immersion, and EUV have to be worked on. These take much more time, funding, and upkeep. Just the spare parts and maintaining personnel can compound the challenges.

The cost of exposing even the most critical layers can be significantly reduced by trading throughput with less columns. This enables resist suppliers to have much less expensive development tools yet with identical exposure characteristics of the HVM tools. Even research labs and research universities can now enjoy low cost, high performance imaging to incubate creativity.

6. CONCLUSION

MEB DW is most attractive in HVM of all layers in a given technology. Such a wide and important application can generate the momentum and funding to develop the technology to extend Moore's Law of scaling and Moore's Law of economy. Maskmaking, prototyping, and HVM of critical layers, will all benefit from the development of this most important application. Increasing the wafer size from 300 to 450 mm offers a golden entry point for MEB DW for all layers. The MEB DW advantage is not limited to the REBL system. There is no reason other MEB DW schemes cannot be geared towards HVM of all layers.

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